LHCb Readout Unit Project

Data merging applications (FEM,RU,L1T) Assessment Criteria

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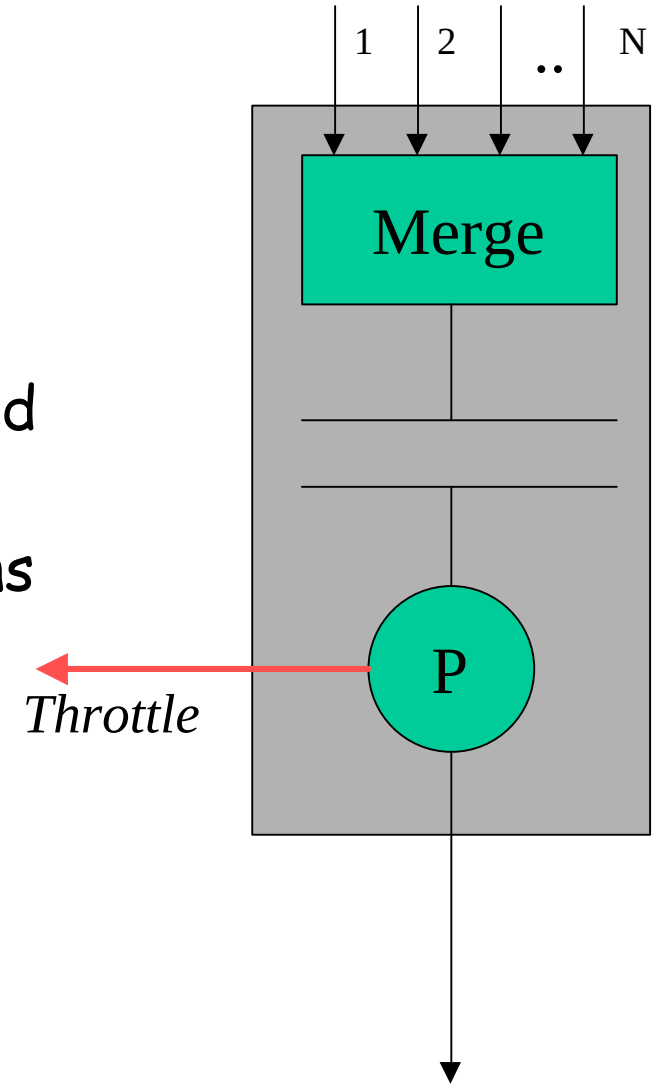
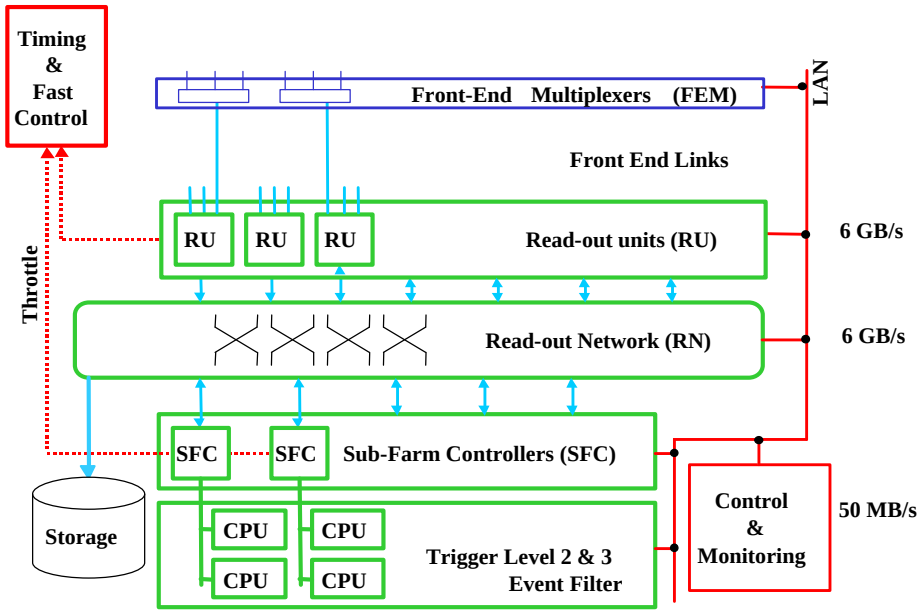
Data Merging

- The Readout Unit is being devised to realise functional components where data are merged
- Typically event data from N links are received, stored, assembled for ordered output as simple sub-events
- Different implementation configurations have been considered to allow for a range of applications



Data Merging in DAQ - FEM

- Subdetector requirements ➡
- FEM works at Level 1 Yes rate
  - 40 kHz -100 kHz
- No output blocking - minimal buffering
  - ~ 1 event
- Output compatible to RU input
- Output should be compatible with input so that multiple levels of multiplexing can be used



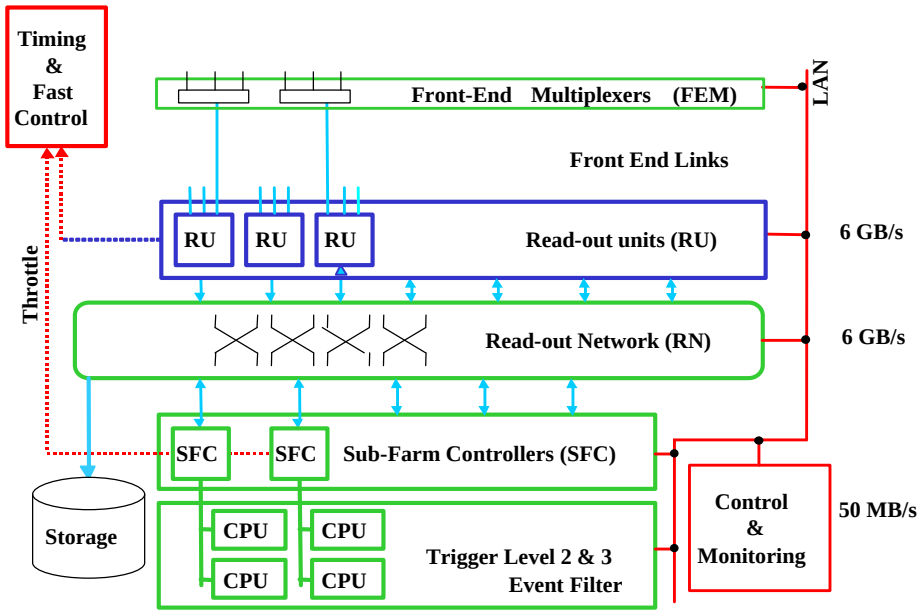
FEMUX - Subdetector Requirements [1)]

	VELO	RICH1	RICH2	IT	OT	SPD/PS	ECAL	HCAL	MUON
No. of input links	100	21	34	108	60	94	188	47	180
Mux Ratio	4:1			4:1		16:1	16:1	16:1	18:1
Data Rate (MB/s)	7	6	9	14	30	4	4	2	3
Unit	FEMUX	-	-	FEMUX	-	CROC	CROC	CROC	Data concen
No of units	25	0	0	27	0	8	14	4	10

- Rate is data rate after multiplexing at 40 kHz
- CALO and MUON use the crate backplane for data concentration
- RICH and OT don't need FEMs (data already sufficiently concentrated)
- VELO and IT need 25 and 27 FEMs respectively, with a mux ratio of 4:1

Data Merging in DAQ – Readout Unit

- Subdetector requirements ➡
- Working at L1 rate 40-100 kHz
- Large event fragments ~250B/input
- Output blocking
- Significant buffering of events
  - ~100-1000 events (~ 1 MB)
- Flow control – throttle to RS
- Format sub-event structure – segmentation and reassembly
- Possibility to implement traffic shaping e.g. constant bit rate
- Flexible determination of destination assignment
  - Simplest round robin, consecutive triggers (spill-over), ….
  - Updates to cope with 'out of service' cpus
  - Support of partitioning



RU - Subdetector Requirements [1)]

	VELO	RICH1	RICH2	IT	OT	SPD/PS	ECAL	HCAL	MUON
No. of links 203	25	21	34	27	60	8	14	4	10
Mux Ratio	4:1	4:1	4:1	2:1	2:1	2:1	4:1	2:1	4:1
No. of RU's 79	7	6	9	14	30	4	4	2	3
Rate/RU (MB/s)	32	44	44	28	34	56	40	34	30

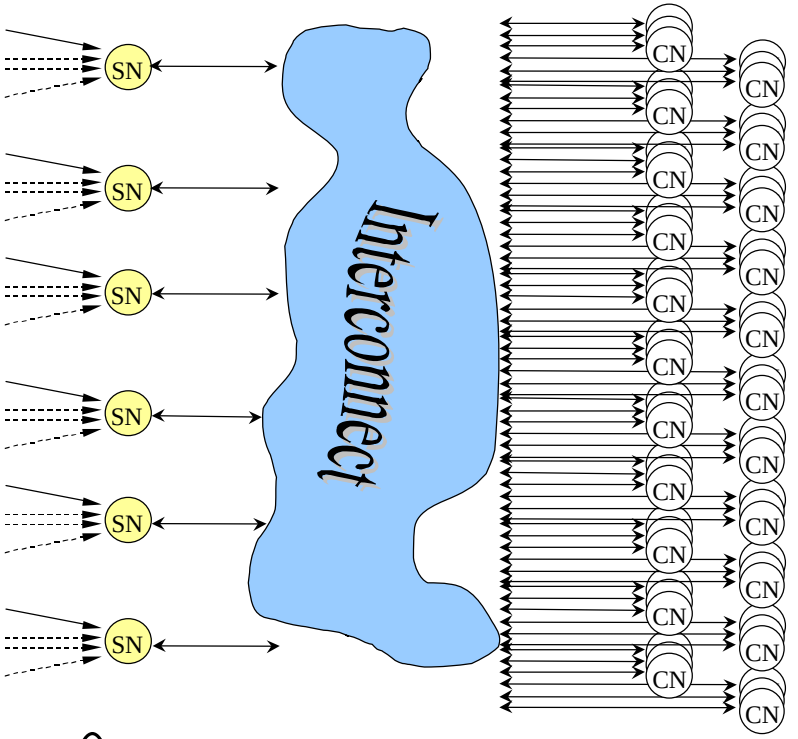
- Assume that the data rate per RU should not exceed 50MB/s
  - Dictated by performance of readout network
- Assumed a L1 rate of 40kHz
  - In case of higher L1 rate will need less FEM's and more RU's

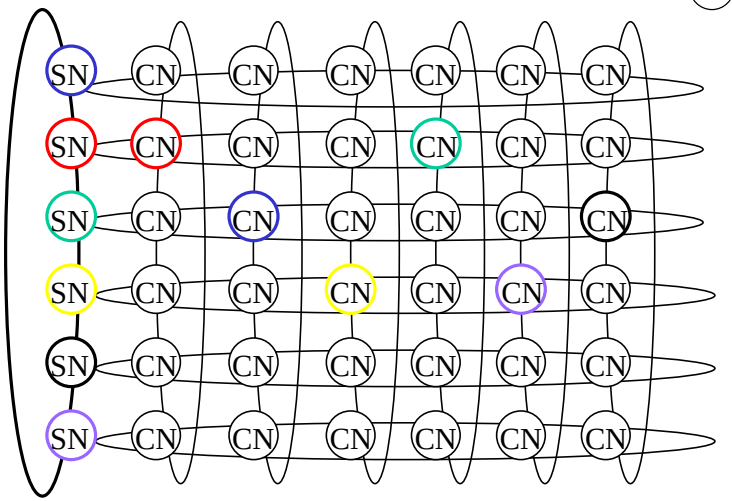
[1)] **lhcb-elec.web.cern.ch/lhcb-elec/html/sub-detectors.htm**

'Overview of front-end electronics in sub-detectors' J. Christiansen

Data Merging in the Level 1 Trigger

- Purpose is to select events with detached secondary vertices
- Algorithm running on ~200 cpus
- Network interconnecting the computing nodes of a processor farm to the data sources
- ~25 sources to a network, currently based on shared memory / torus topology
- Working at Level 0 Yes rate ~1.1 MHz
- Latency restrictions (~10's μsec)
- Small event fragments (~30B avg)
- Medium buffering (~10-100 events)
- Output to network card (NIC)
- Possible output blocking
- Flow control – throttle to TFC





Assessment Criteria

- Functionality assessed against functional requirements
  - Including environment requirements (space, power, …)
- Performance assessed against performance requirements
- Cost – assessed against overall absolute cost
  - planned RU budget : 1 M SFr, 110 modules @ 9 kSFr / module
- System-based acceptance test, problem diagnosis
- Support for system integration and commissioning, long-term consolidation
- Flexibility – assessed against unforeseen requirements (new running modes, protocols, upgrades,…)
- Maintenance and Support – managing component obsolescence, possibility to support and adapt over lifetime
- Generality - range of applicability in LHCb (scope)
  - Cost/benefit of single vs multiple moduletype
- Commonality – use in more than 1 experiment

Input information to review

- Description of design process
- Design features and description of board layout – support for:
  - Readout protocols and data formatting
  - Event fragment rates and buffer capacity
  - Error detection and reporting, flow control
- Results of simulation studies
- Results of prototyping – test procedures and performance measurements
- System implementation details – space, power, cooling
- Potential future work programme
  - Effort/resources to finalise design and produce final boards
  - Participation in small scale tests and full-scale commissioning
  - Schedule for module production, testing, commissioning
- Cost estimate