Control requirements from sub-detectors

Results of the ECS to front-end interface questionnaire

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Response

- Questionnaire has gone out in November.
- First results presented in December LHCb week.
- Reactions from all sub-detectors and some other ‘sub-systems’:
  - full answer from all sub-detectors except:
    - inner tracker (‘*too early*’ *11/1999*)
    - DAQ
  - full answer from Readout Unit and magnet.

Response

- Thanks !
- Remember:
  this is the situation of November 1999
- If you have updates or more information since then, please let us know!

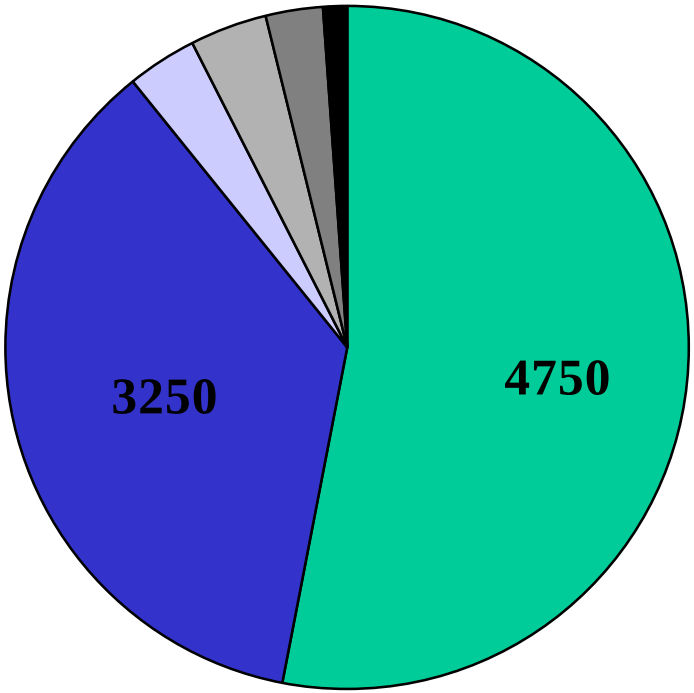
Results

ECS tasks:

- initialisation
- loading parameters
- loading FPGA’s
- status monitoring
- calibration
- debugging

Some Numbers

- Some ideas concerning number of boards and crates:
- on/near detector: >8000 boards (Outer tracker, Muon)
- behind the wall: ?



Some Numbers

- on/near detector: >150 crates
- 9U, VME

  but:
- Only for mechanics and power supplies, no need for the VME bus

Technical Aspects

Interfacing:

- I2C (configuration of chips)
- JTAG (loading of FPGA's, board testing, parameter loading)
- no other 'definitive' choices,

– but a lot of suggestions and/or investigations:

  - PCI, serial, CAN, I/O lines, ...

Technical Aspects

‘On Board Intelligence’:

- Some CPU and/or FPGA availability

Selftest:

- JTAG
- write+readback tests

No very strong space/radiation etc. constraints (yet).

Functionality and Performance

Typical configuration:

- 1 up to few hundred bytes/board

LookUp Tables:

- few up to few hundred kbytes/board

FPGA loading:

- few hundred kbytes up to few Mbytes

– some boards maybe grouped

Functionality and Performance

Time constraints:

- FPGA downloads > 1 min.
- LUT loading ~seconds (< 1min)

- loading in general only necessary once per run or fill.

Functionality and Performance

Monitoring:

- very few active monitoring (yet)
- small amounts of data (few bytes)
- infrequent dumps of data (order of Mbytes)
- readback to detect single event upsets

Functionality and Performance

Other:

- *calibration* mode:
  - threshold and testpulse runs
  - synchronisation with DAQ needed
- board tests
- *'reset'*

Conclusions

- *'classical'* Fieldbus cannot do the job.
  - Ethernet could.
- No need for VME bus.
  - But grouping of boards is likely i.e. need for *'crate controller'* or *'fan-out'.*

Conclusions

	Boards	I2C	JTAG	Other	'Fan-Out'	Param./ Board	Config./ Board
Vertex	110	Y	Y			2.5 kb	1-10 Mb
Outer Tr.	4750		Y		Y	2 b - 0.5 kb	
RICH	300	Y	Y			10 kb	10 Mb
Calorim.	300			Serial	Y	800 kb	Mb
Muon	3250	Y	Y	I/O, ser.		10 b - 100 kb	Mb
RU	200	Y	Y	PCI			100 kb