LHCb Technical Board 20 March 2003

Agenda

1. **Approval of last TB summary**
2. **L1 Trigger**

Situation	**W. Witzeling**
Actions and Planning	**H. Dijkstra, B. Jost**

3. **Planning for the Light and Trigger TDRs** — **all**
4. **Report on the CARIOCA Review** — **J. Christiansen**
5. **Approval of Milestones Document Vers 2** — **W. Witzeling**
6. **Milestone follow-up (review/preview)** — **W. Witzeling**
7. **Status of system schedules** — **R. Lindner / all**
8. **Summary of Installation Review** — **R. Lindner**

Participants: N. Brook, J. Christiansen, H. Dijkstra, W. Flegel, R. Forty, B. Jost, D. Lacarrere, R. Lindner, T. Nakada (phone, point1-3), W. Riegler, T. Ruf, O. Schneider, A. Schopper, A. Smith, O. Steinkamp, O. Ullaland, W. Witzeling

Excused: G. Carboni, J. Lefrançois, C. Matteuzzi, A. Pellegrino, B. Schmidt, U. Straumann, D. Websdale

1. **Approval of last TB summary:** The summary of the TB on 27th February 2003 was approved with a few comments. Concerning the 'sticky charge' defect it was stated that this fault will be cured in the next version of the Beetle chip.
2. **Level 1 Trigger:**
   Situation: W. Witzeling reported that the LHCb management had met V. Lindenstruth to discuss the future involvement of the Kirchhoff Institute Heidelberg in the L1 Trigger project. The original scope of the L1 Trigger project matched very well the KIP profile. Since then the requirements for the L1 Trigger have significantly increased (e.g.: the number of CPUs increased from ~120 to ~700 or more) and

V. Lindenstruth concluded that the project had become too large for KIP to handle alone and that they no longer wished to have responsibility for the project.

V. Lindenstruth concluded that KIP cannot keep anymore the responsibility for this project. The KIP group will conclude their work on the L1 trigger prototype and publish a final report. Nevertheless, his group will assist with their knowledge for the near future as far as resources are available.
Action and Planning: H. Dijkstra presented the next steps concerning the L1 Trigger project towards the Trigger TDR. A status report on a combined DAQ/L1 implementation is scheduled for the 16th of April 2003, followed by a review on the 29th of April 2003 that will include four external referees. A review report will be available before the next LHCb week in May 2003. The L1 trigger baseline implementation as it will be described in Trigger TDR will use the information from L0DU, VELO and TT

with a maximum output rate of 40MHz. The costs will be based on this baseline implementation including the potential to extend the scope for L1.
B. Jost reminded the TB of the DAQ architecture as described in the Online TDR and explained the proposal for a combined DAQ/L1 Trigger architecture. The exact costs for this solution can only be evaluated once the L1 data sources are defined. The present estimation indicates, that the costs for the baseline solution should be within the value given in the Online TDR plus approximately 1 MCHF.
The TB encouraged the DAQ and Trigger groups to continue their effort in view of a combined DAQ/L1 farm and requested to come forward with an elaborated proposal to be presented during the review scheduled for the 29th of April 2003.

3. **Planning for the Light and Trigger TDRs**: T. Nakada presented the table of contents for the LHCb 're-optimization' TDR that should not exceed 100 pages, it will be a self-contained document. The key dates for the preparation of the LHCb 're-optimization' TDR and the Trigger TDR have been discussed and the TB agreed on the following schedule:

LHCb reoptimization TDR

23 June	Overview, VELO, Tracking, PID chapters delivered
26 June	Physics performance chapter delivered
4 July	Semi-complete draft sent to TB
8 July	TB discussion
14 July	RICH1, TT, Beam Pipe, Cost and Schedule chapters delivered
21 July	First complete draft sent to TB
23 July	TB discussion
7 August	Second draft sent to TB
11 August	TB discussion
18 August	Final draft released to the collaboration
1 September	Deadline for comments from collaboration
9 September	TDR sent for printing

Trigger TDR

27 June	First complete draft sent to TB
7 July	TB discussion
18 July	Second draft sent to TB
24 July	TB discussion
4 August	Final draft released to the collaboration
1 September	Deadline for comments from collaboration
9 September	TDR sent for printing

LHCb week 15-19 September
LHCC 24-25 September

4. **Report on the CARIOCA Review**: J. Christiansen reported on the outcome of the review of the CARIOCA front-end chip (for the muon MWPCs). The oscillation problem has been cured by a adding a capacitor as dummy load to the differential input. However, the different detector configurations result in a large variation of detector capacitance.

Consequently this requires the production of four types of FE boards, each with a different capacitor. The last version of the CARIOCA seems to be 95% functional and has already been used for chamber readout. Nevertheless, the remaining problems have to be solved, tests of packaged chips and systematic simulation of well-defined worst-case conditions must be performed. The latest version of CARIOCA has been submitted in February 2003 and is expected to arrive back in May 2003. This will not leave much time for testing and possible design changes before the next submission in June 2003. The schedule looks extremely tight.

5. **Approval of Milestones Document Version 2:** Following the approval of the Inner Tracker TDR and the addendum to the Muon TDR the LHCC milestones for the IT and the MWPC production have been added into the milestone document. Also, the status of milestones has been updated. The revised version of the document can be found at:
   https://edms.cern.ch/document/356577/2
   The TB approved the LHCb Milestones Document Version 2.

6. **Milestone follow-up (review/preview)**: W. Witzeling presented the preview list of milestones and reminded the project leaders that, in case of a missed milestone, an action plan has to be established that allows catching up with the original schedule. The status of the milestones between April 2002 and September 2003 has been reviewed (see annex). There are presently three failed milestones:
   1. Photon detector: bump bonding issue
   2. Reception of coils and yoke: intentionally delayed to achieve just-in-time delivery (expected June 03)
   3. ECS electronics prototype interfaces ready (expected June 03)

   The latter may have also an impact on the next ECS milestone in September 03, but should not influence the milestones thereafter.

7. **Status of system schedules:** W.Witzeling stated that it becomes now urgent to establish a consistent set of schedules for LHCb. To this aim the system schedules have to be coordinated with the LHCb installation schedule. The project leaders are responsible for having a system schedule established and internally approved by the detector groups by the next LHCb week in May 2003. R. Lindner reminded the TB that the schedules have to follow the guidelines given in the document 'Schedule and Milestones' and they will then be approved following the procedure described therein (https://edms.cern.ch/document/369653/1).

8. **Summary of the Installation Review**: R. Lindner summarized the LHCb installation review held on the 13th March 2003. The summary including comments and question from the reviewers can be found at:
   Summary of Installation Review

Next Technical Board (LHCb Week)

Friday 23 May 2003 at 14:00 in room 160-1-009

System	Subsystem	Milestone	Planned Date	Achieved Date	Expected Date	Comment
RICH	Photondet	Working 40MHz pixel readout chip	June-02	June-02		
DAQ	ECS	ECS software framework first release	June-02	June-02		
VELO	Electronics	Test of hybrids(Beetle1.1+SCTA_VELO)	October-02	October-02		
RICH	Photondet	Working HPD with 10MHz readout	December-02			pending (bump bonding)
VELO	Mech/Vac	Engineering Design Review with LHC group	January-03	January-03		
CALO	HCAL Mech	10% of mechanics assembly	February-03	December-02		Ahead of time
VELO	Silicon	Design review	February-03	February-03		
VELO	Electronics	FE chip review and decision	March-03	January-03		
MAGNET	Magnet	Reception of coils and yoke	March-03		June-03	just-in-time delivery
DAQ	ECS	ECS electronics interfaces prototypes ready	March-03		June-03	delayed
MUON	MWPC	Engineering design completed	April-03			EDR on 16 April 03
VELO	Electronics	Final prototype of digitizer board	May-03		July-03	delayed (common L1 board)
Outer Tracker	Module	Engineering design completed (EDR)	May-03			EDR on 15 April 03
RICH	R2mechopt	Production drawings completed	May-03			looks okay
VELO	Silicon	Production Readiness Review	June-03			planned for June 03
IT	Project	Final decision on production site(s)	June-03			looks okay
IT	RO links & SB	Full prototype test of readout link	June-03			looks okay, radiation test!
CALO	SPD/PS Mech	start of serial production	June-03			looks okay
MUON	Inner-M1	Technology choice	June-03			Rad test end May '03
MUON	Electronics	Full chain electronics test completed	June-03			looks okay
DAQ	TFC	TFC prototypes ready	June-03			design finalized March
CALO	ECAL Mech	50% of stack assembly	July-03	December-02		Ahead of time
VELO	Electronics	Pre-production run	July-03		September-03	delayed (common L1 board)
Outer Tracker	Electronics	Validation of baseline option (OTIS)	July-03			
RICH	R2mechopt	Orders for mirrors & superstructure placed	July-03			
MUON	MWPC	Begin chamber production	July-03			
VELO	Silicon	Order 50% of sensors	August-03			
RICH	Photondet	Prototyping 40 MHz HPD completed	September-03			
RICH	Aerogel	Decision on aerogel parameters	September-03			
MAGNET	Installation	Assembly terminated	September-03			
MUON	Electronics	CARIOCA review & decision on FE chip	September-03			
MUON	Electronics	DIALOG design and test completed	September-03			
MUON	Electronics	SYNC design and test completed	September-03			
DAQ	ECS	ECS electronics interfaces finalize design	September-03			potentially delayed