A Rad-Hard Slow Control Network for the CMS Central Tracker

A. Marchioro,
G. Cervelli, F. Faccio, K. Kloukinas, C. Ljuslin,
P. Moreira, E. Murer, C. Paillard, F. Vasey
CERN-EP

Outline

- Motivations and Requirements
- Architecture
- Network and system components:
  - Token-Ring Network
  - Local Monitoring
  - Timing and Trigger Distribution
- Network: High level protocol
- Project Status

Motivations

- Requirements and Architecture no different from traditional slow control system
- Merging with timing distribution: unusual !
- Commercial rad-hard control components exist, but not suitable for application and expensive
- Special concern: reliability and SEU robustness
- Looked at commercial networks:
  - Ethernet
  - Mil1553
  - CANbus
  - IBM Token-ring
  - JTAG
  - Other Field-buses …

Either too complicated, or don't work in magnetic fields or unsuitable or too expensive, or…

Requirements

- Must carry data and 40 MHz clock for system synchronization
- Bi-directional
- 150m optical + ~10 m copper
- Compatible with opto-electronics used for data read-out
- Redundancy
- Low digital noise
- Easy interfaces on the FE ASICs
- ~120,000 FE ASICs, ~20,000 MCMs, ~2,000 controllers, ~200 links, ~50 control boards in Countingroom
- Low cost (node price < 100 $)

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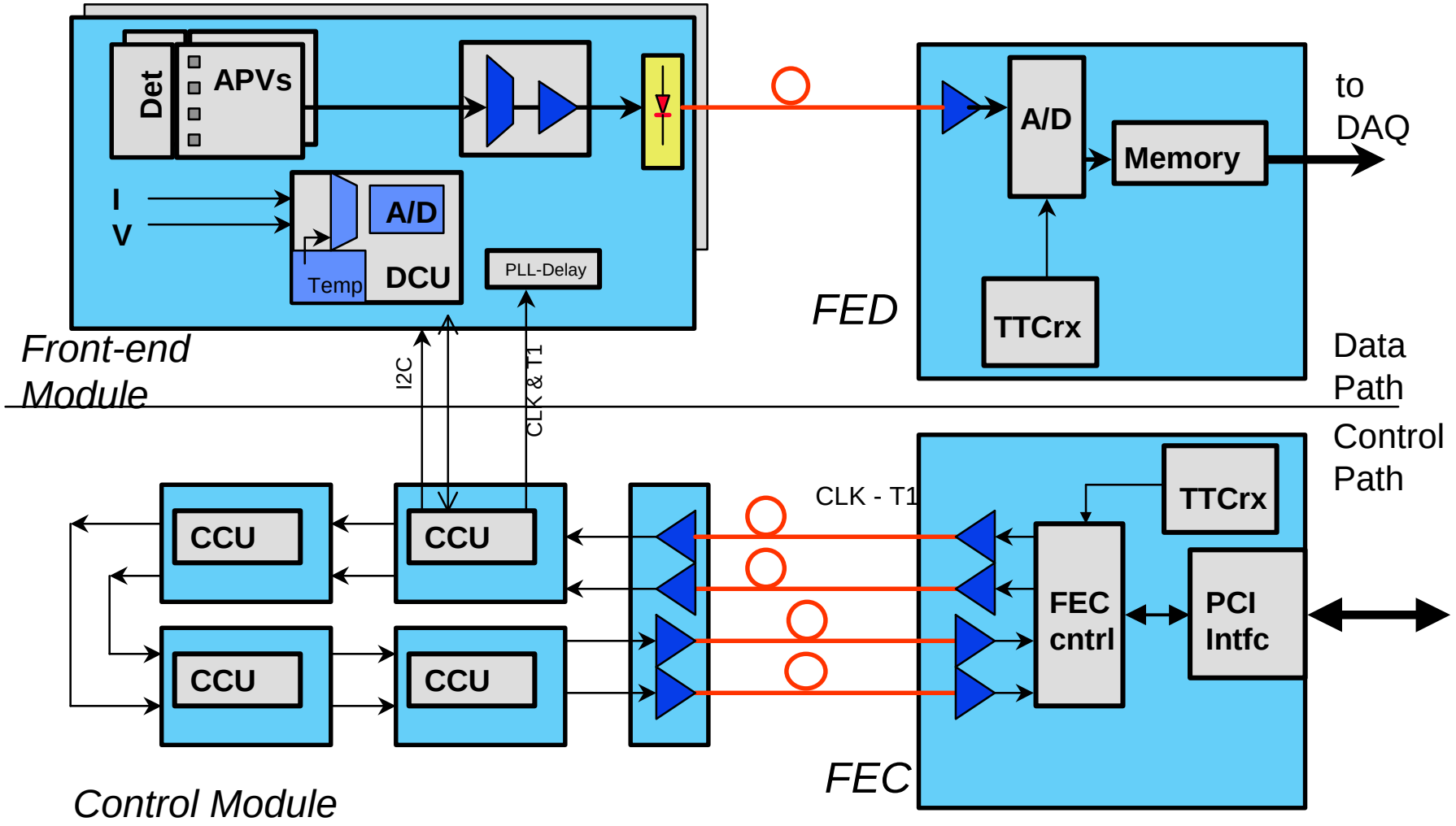
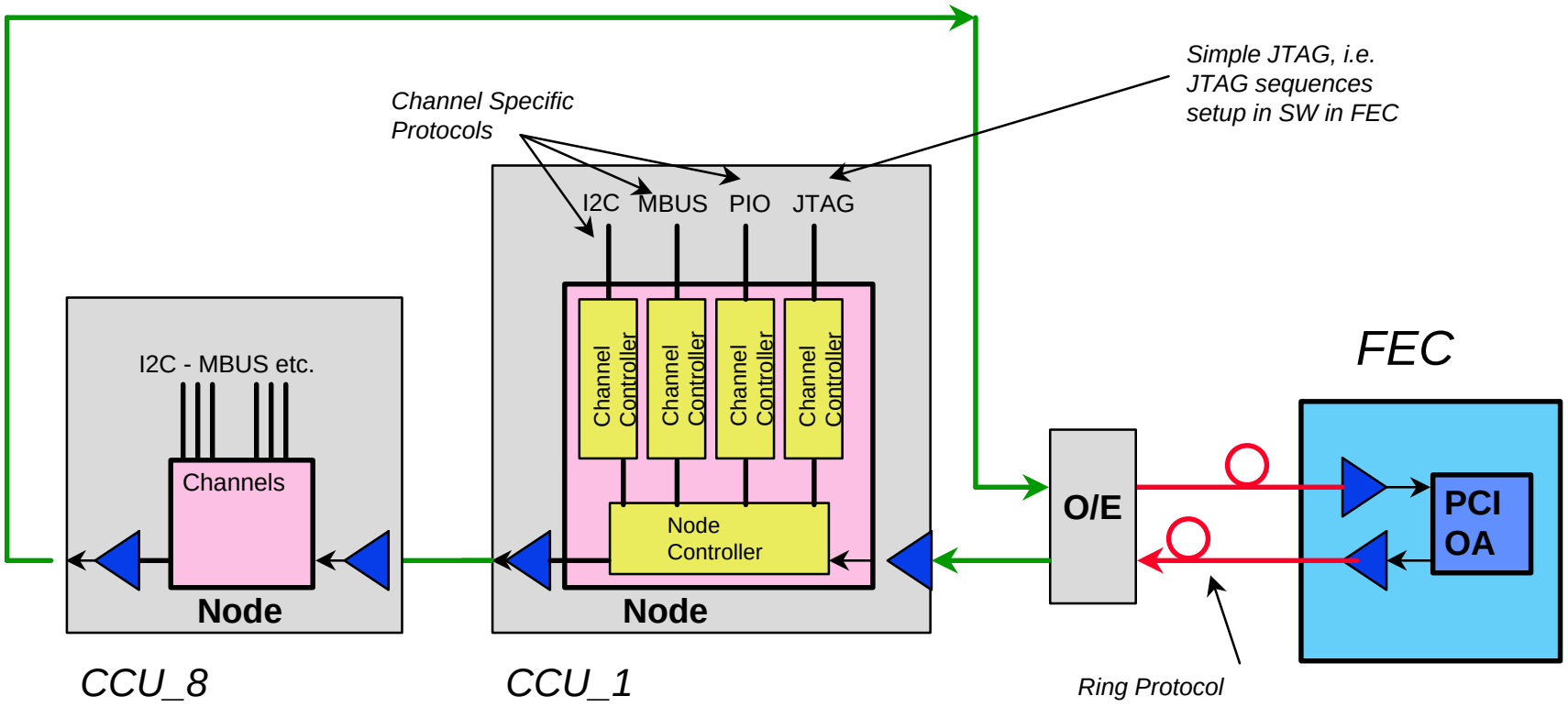
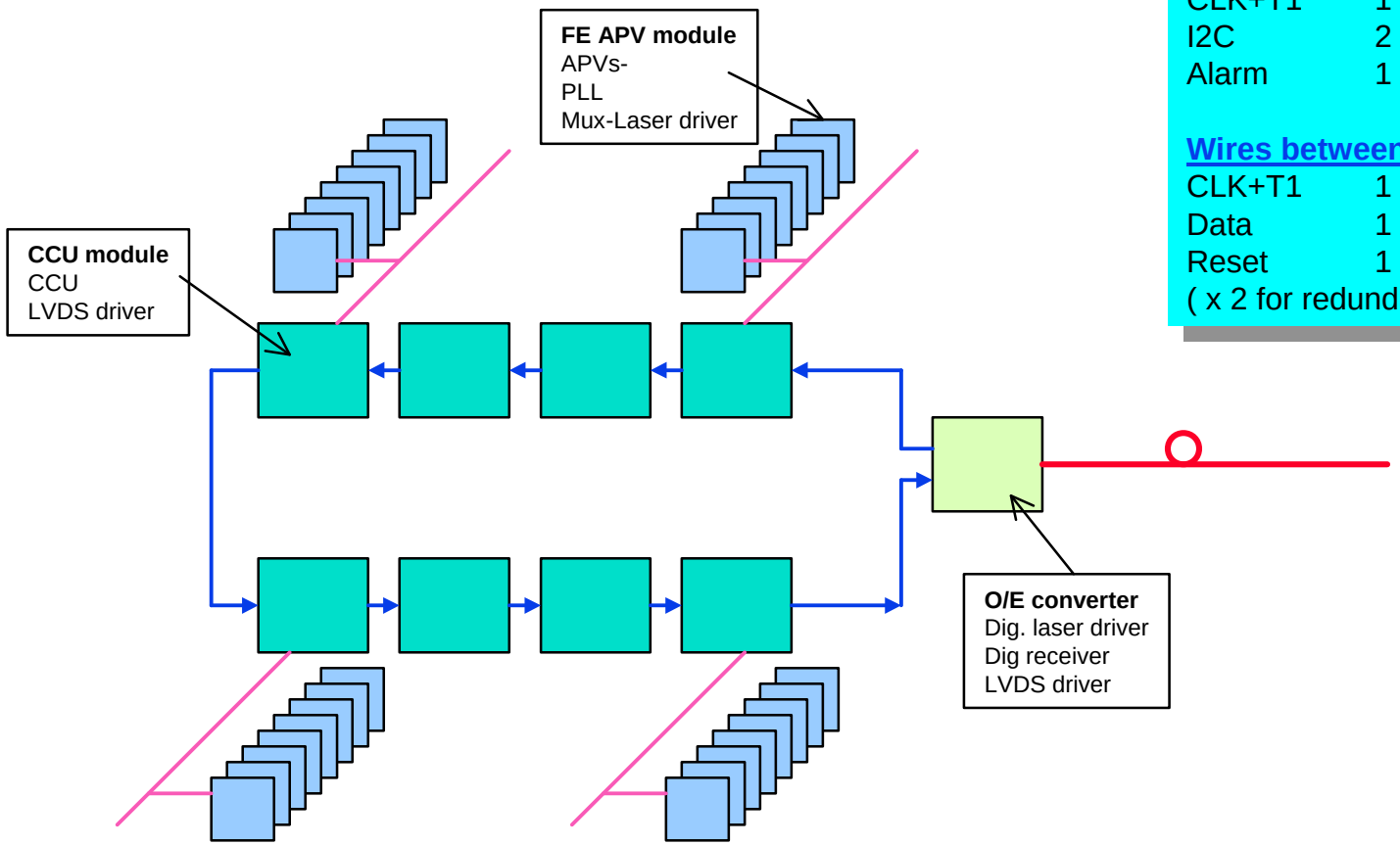
CMS Tracker R-O: General Architecture



Logical View of Control Ring



Full control ring



Wires between CCU and FE modules

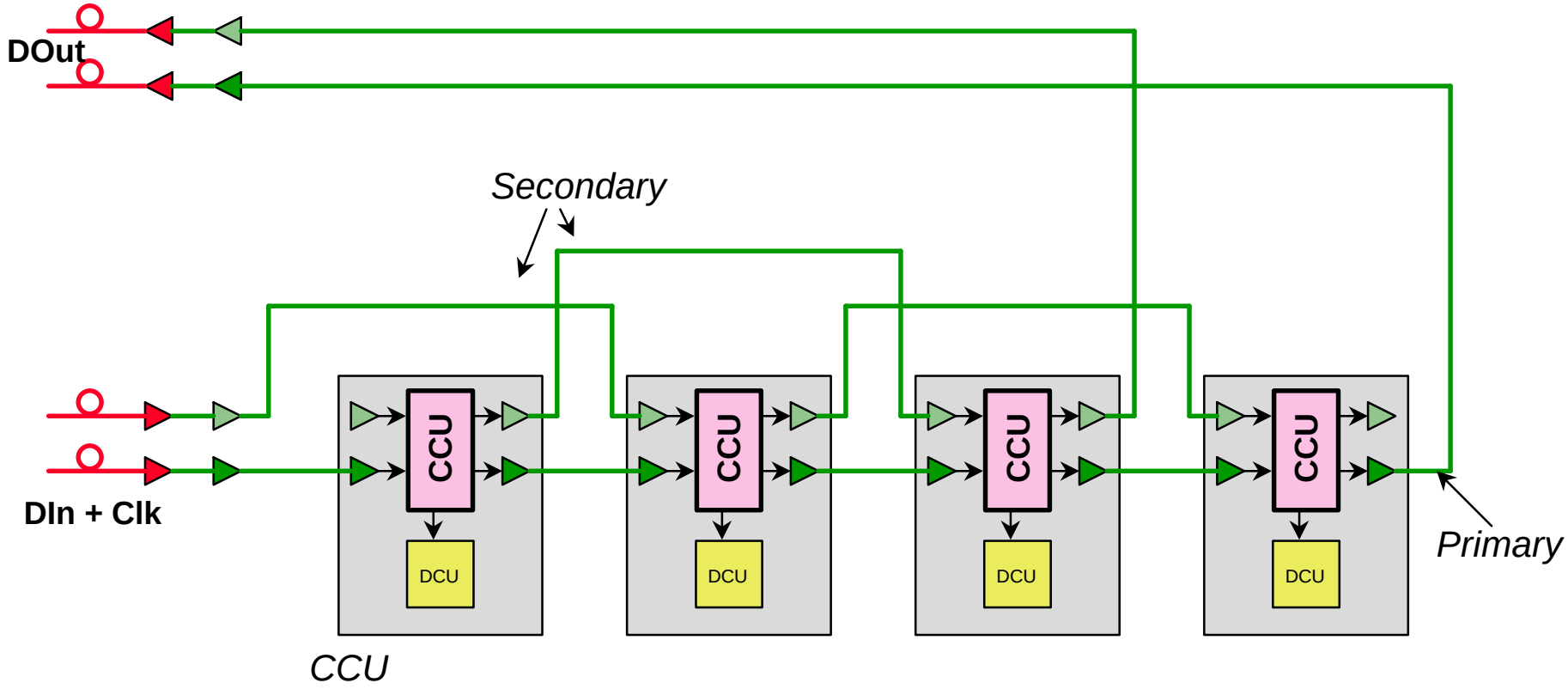
CLK+T1	1 * diff pair	(LVDS)
I2C	2	(TTL OC)
Alarm	1	(TTL OC)

Wires between CCU modules

CLK+T1	1 diff pair	(LVDS)
Data	1 diff pair	(LVDS)
Reset	1 wire	(TTL)

(x 2 for redundancy)

“Module Skip” Redundancy



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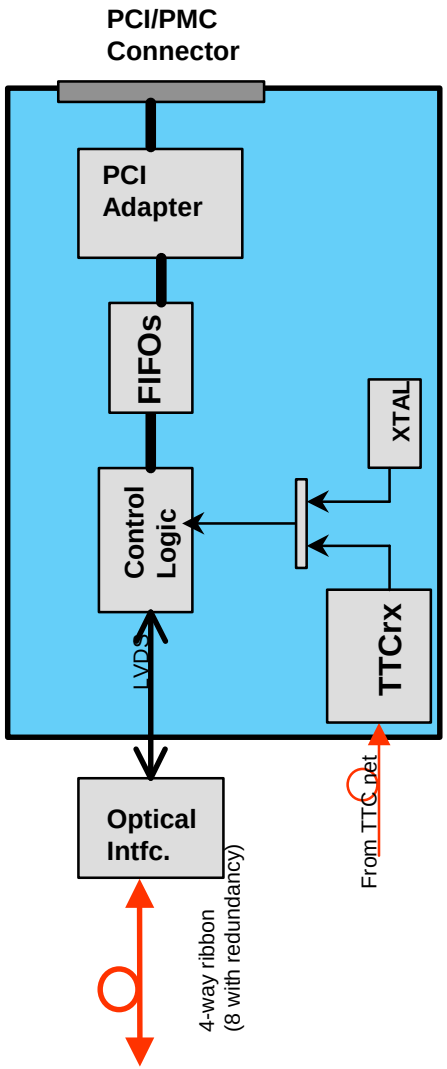
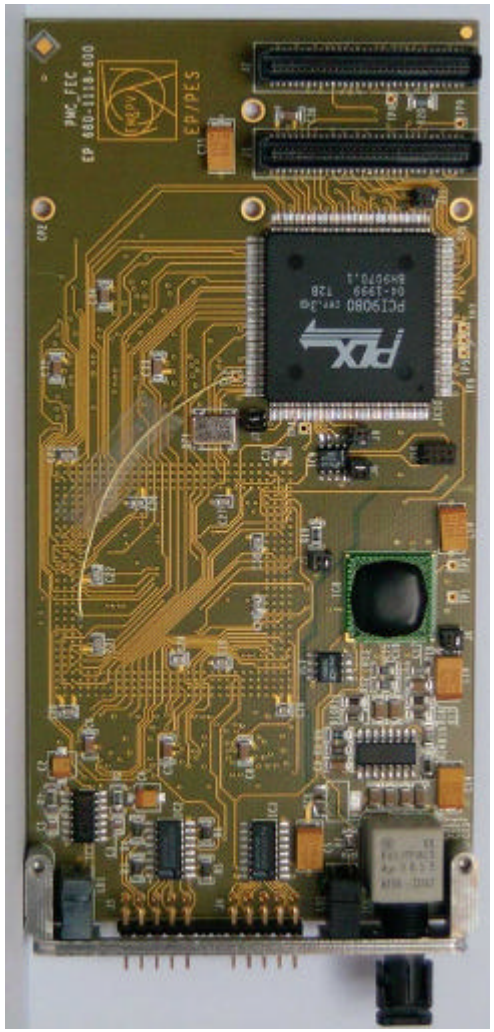
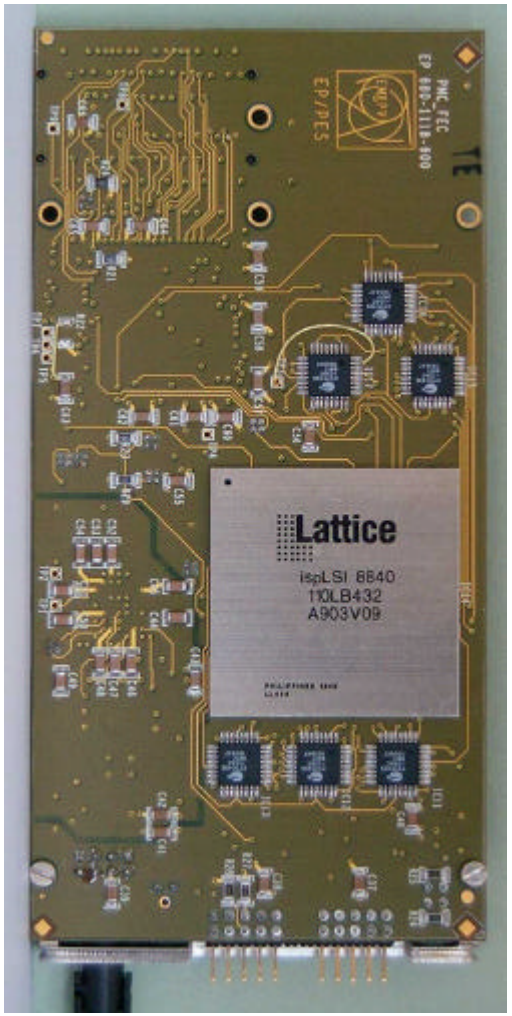
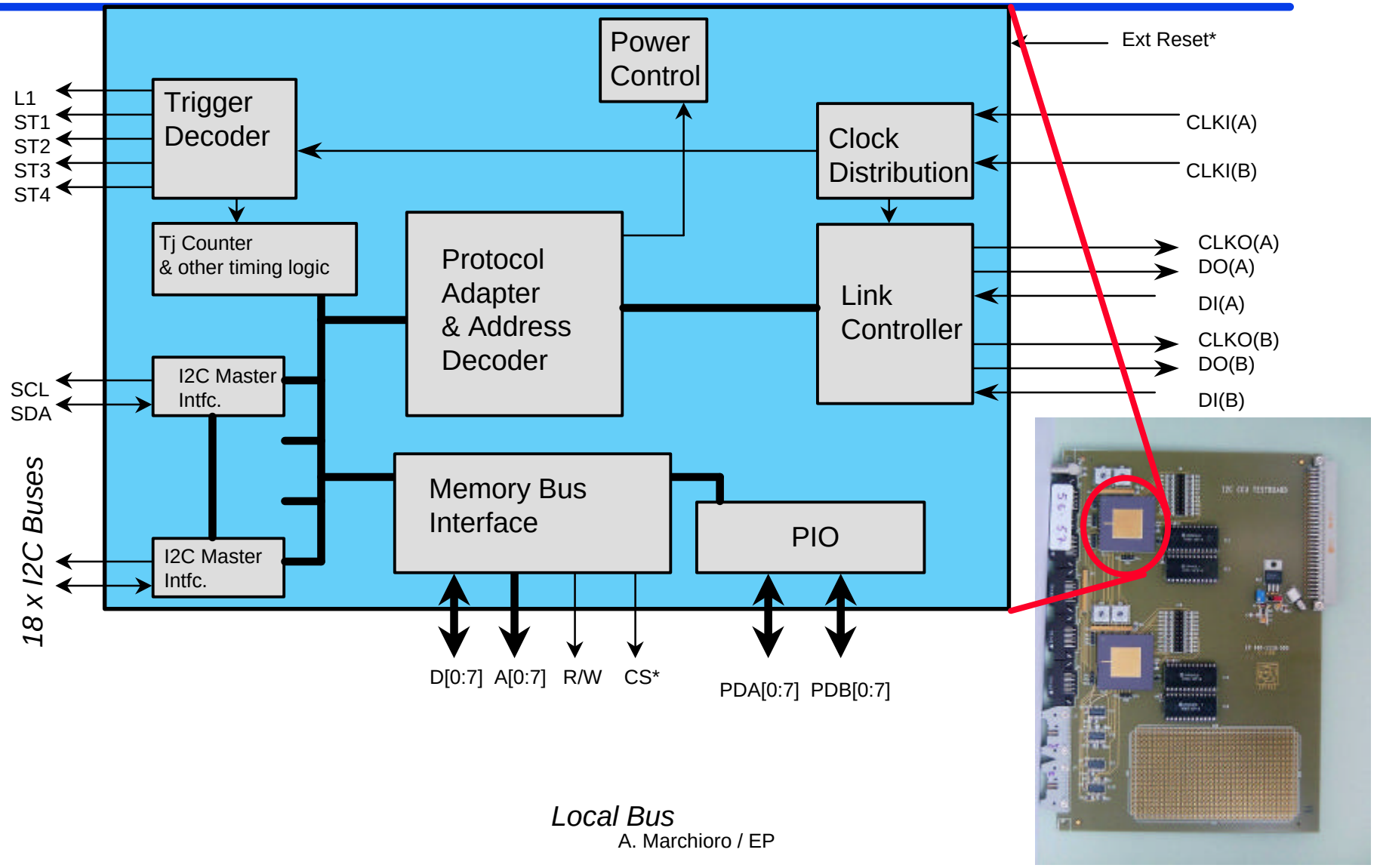
FEC: Front-End Control Board





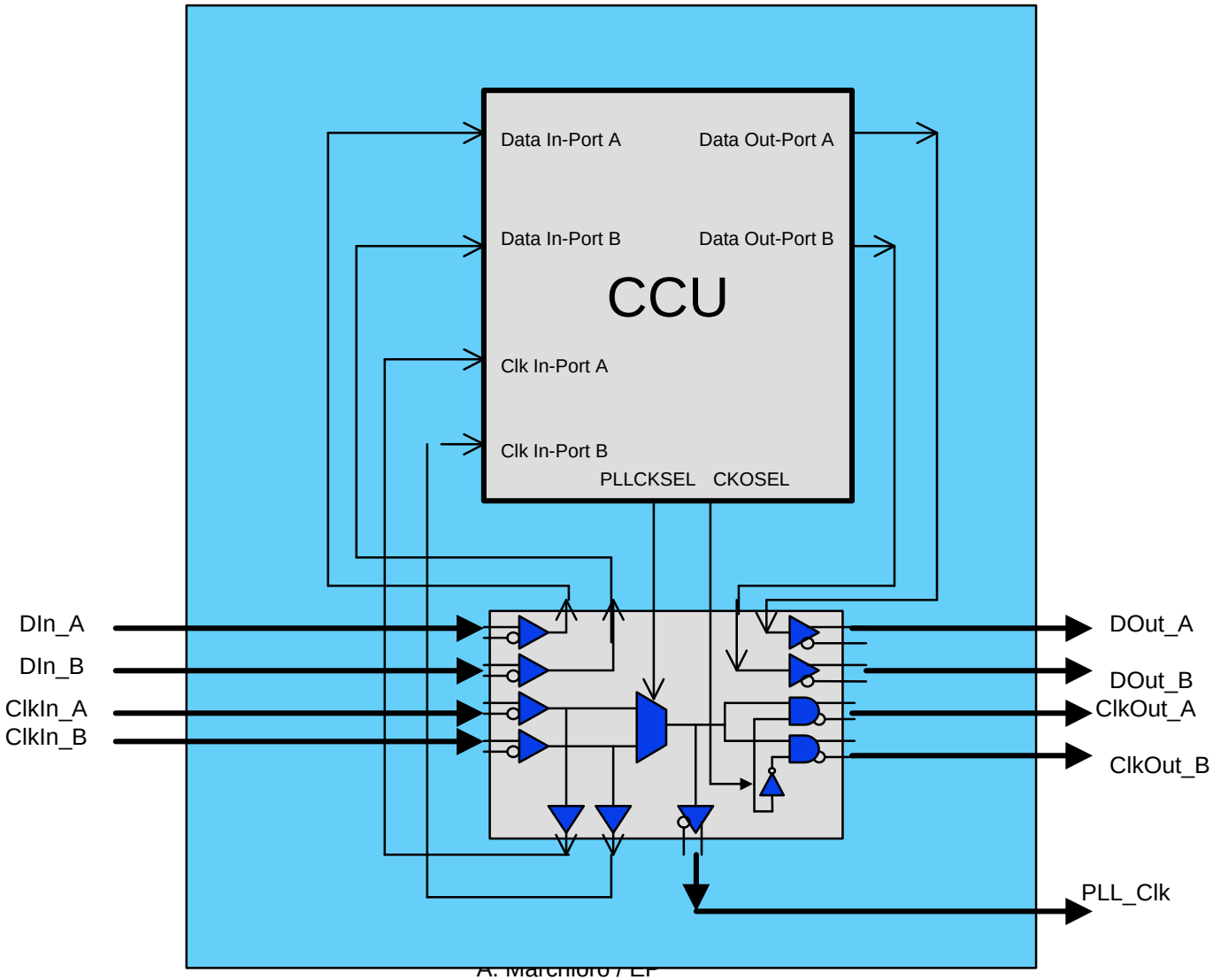


CCU: Communication and Control Unit

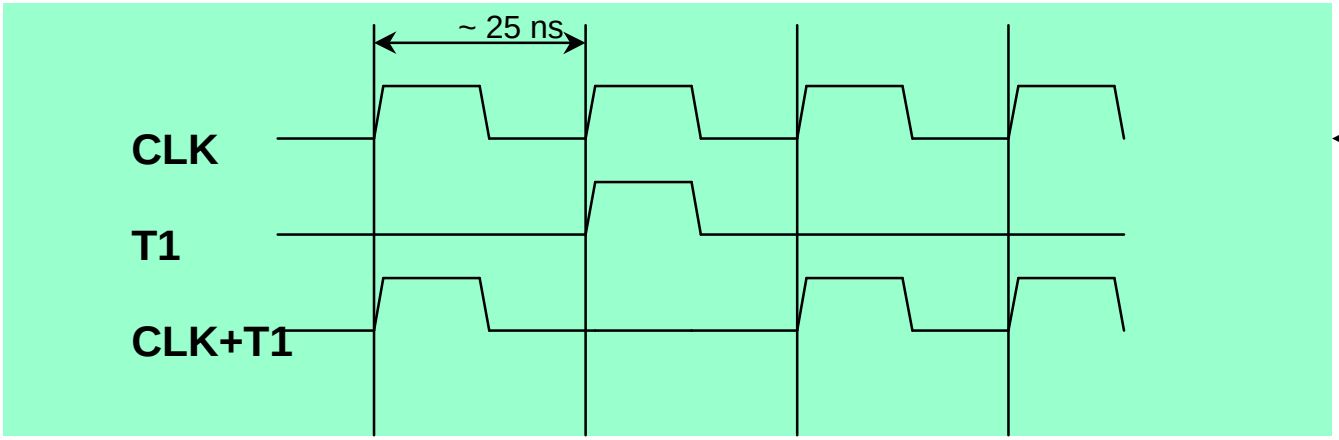


Local Bus

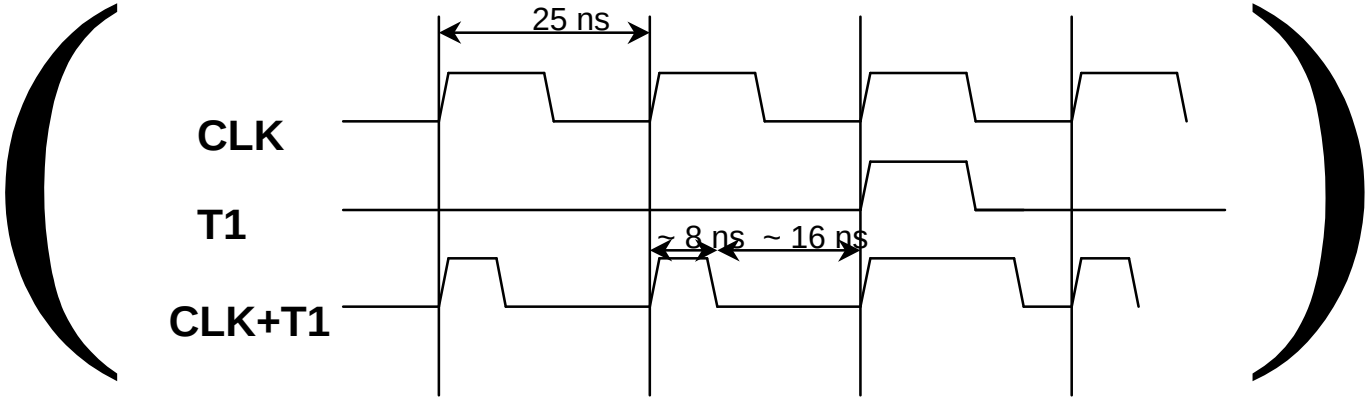
CCU-M Cabling With Redundancy



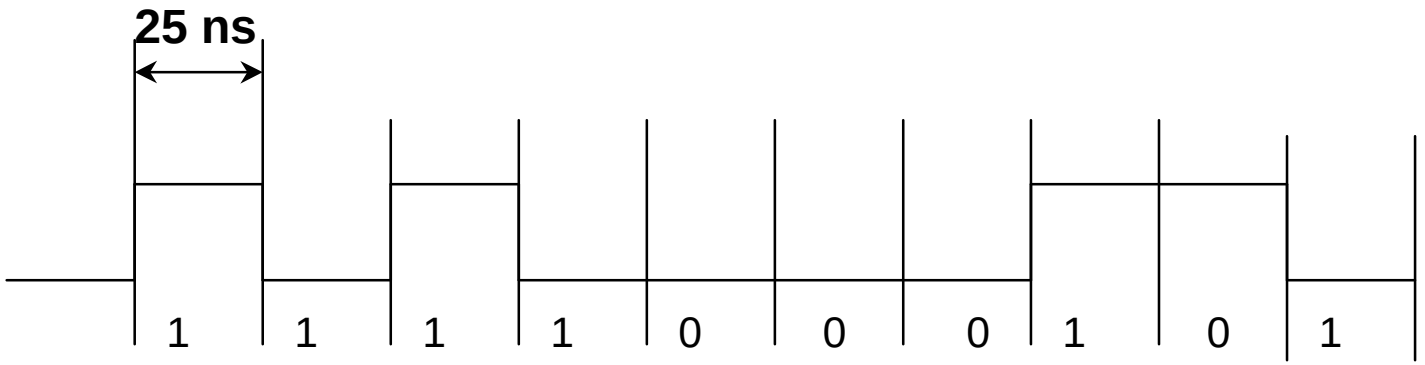
Coding of Clock and T1: Two Options



Used

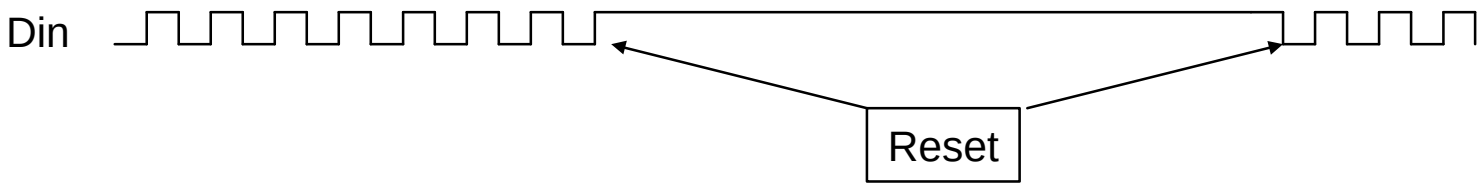


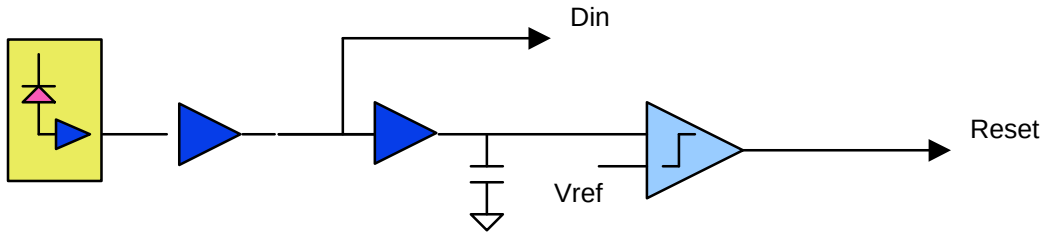
NRZ_I (Invert 1 on Change) Coding



- “0” : no transitions (< 3 conseq.)
- “1” : transition at start of cycle

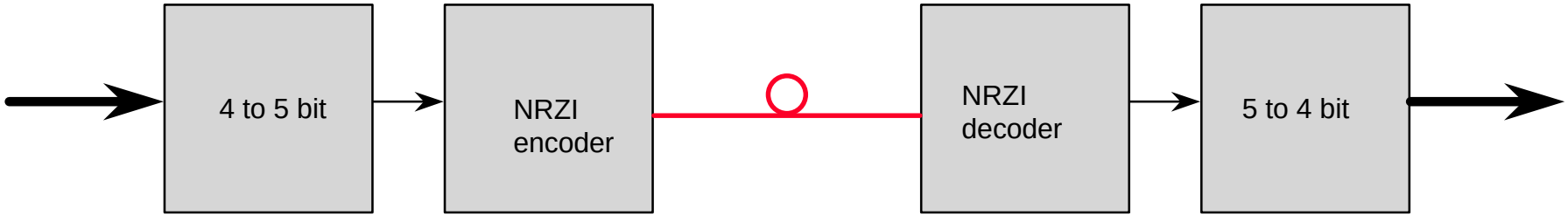
Hard Reset (i.e. how to get always out of troubles)





- Power-Up reset only must be avoided
  - use long sequence of 1's (invalid data sequence) in data stream
  - extra comparator in receiver ASIC

4-5 Bit Encoding

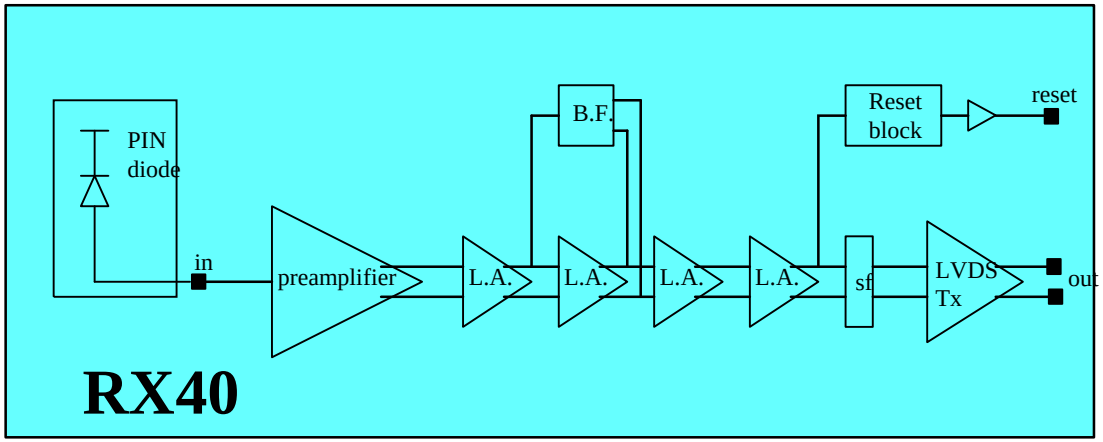


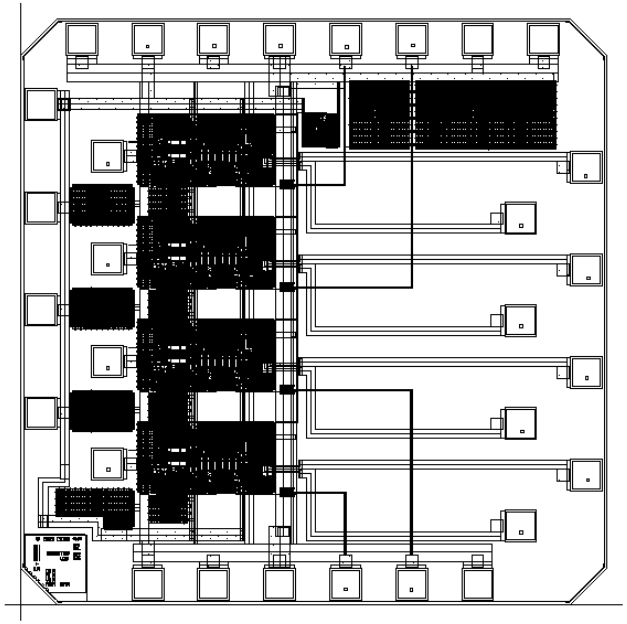
4 bit Binary	Hex	5 bit Symbol
0000	0	11110
0001	1	01001
0010	2	10100
0011	3	10101
0100	4	01010
0101	5	01011
0110	6	01110
0111	7	01111
1000	8	10010
1001	9	10011
1010	A	10110
1011	B	10111
1100	C	11010
1101	D	11011
1110	E	11100
1111	F	11101

Control Symbol	Code	Comment
Idle	11111	Idle
J	11000	In SOF field
K	10001	in SOF field
H	00100	Special
R	00111	Reset
S	11001	Set
T	01101	Termination

Other network components

- RX40: a RH 80 MHz BW digital receiver with Automatic Gain Control
- Laser Driver: a RH Linear driver for analog and digital data

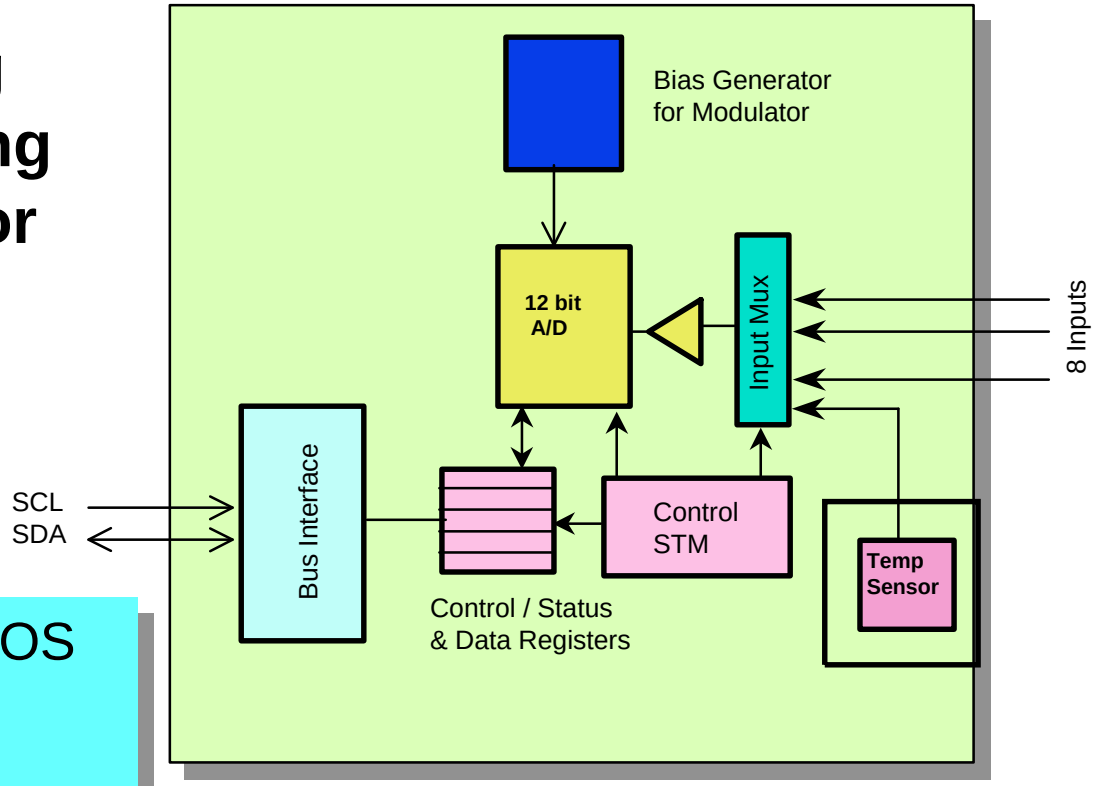




Exists already

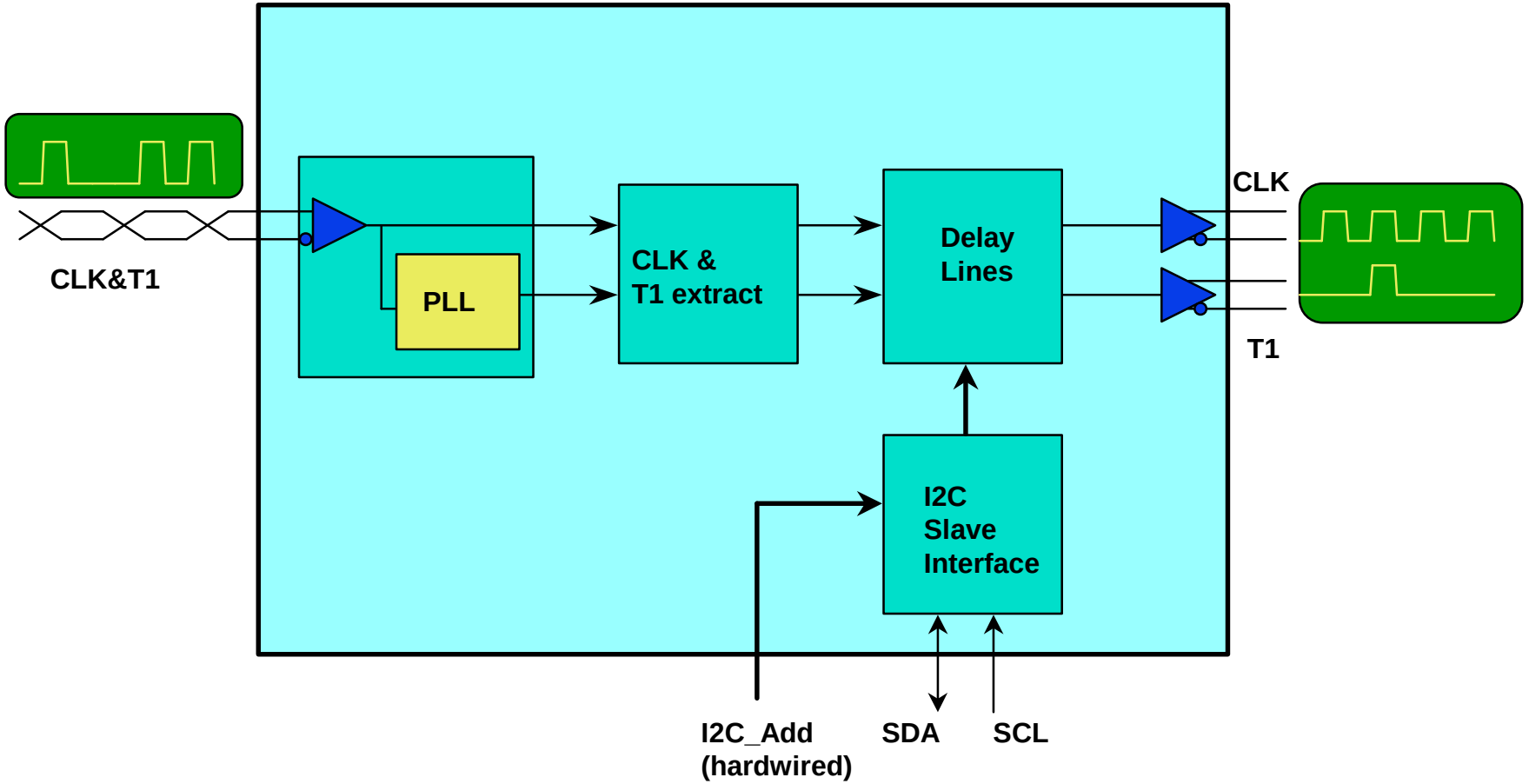
DCU: Detector Control Unit

- **Local Monitoring**
  - ✓**Current Sensing**
  - ✓**Voltage Monitor**
  - **Temperatures**

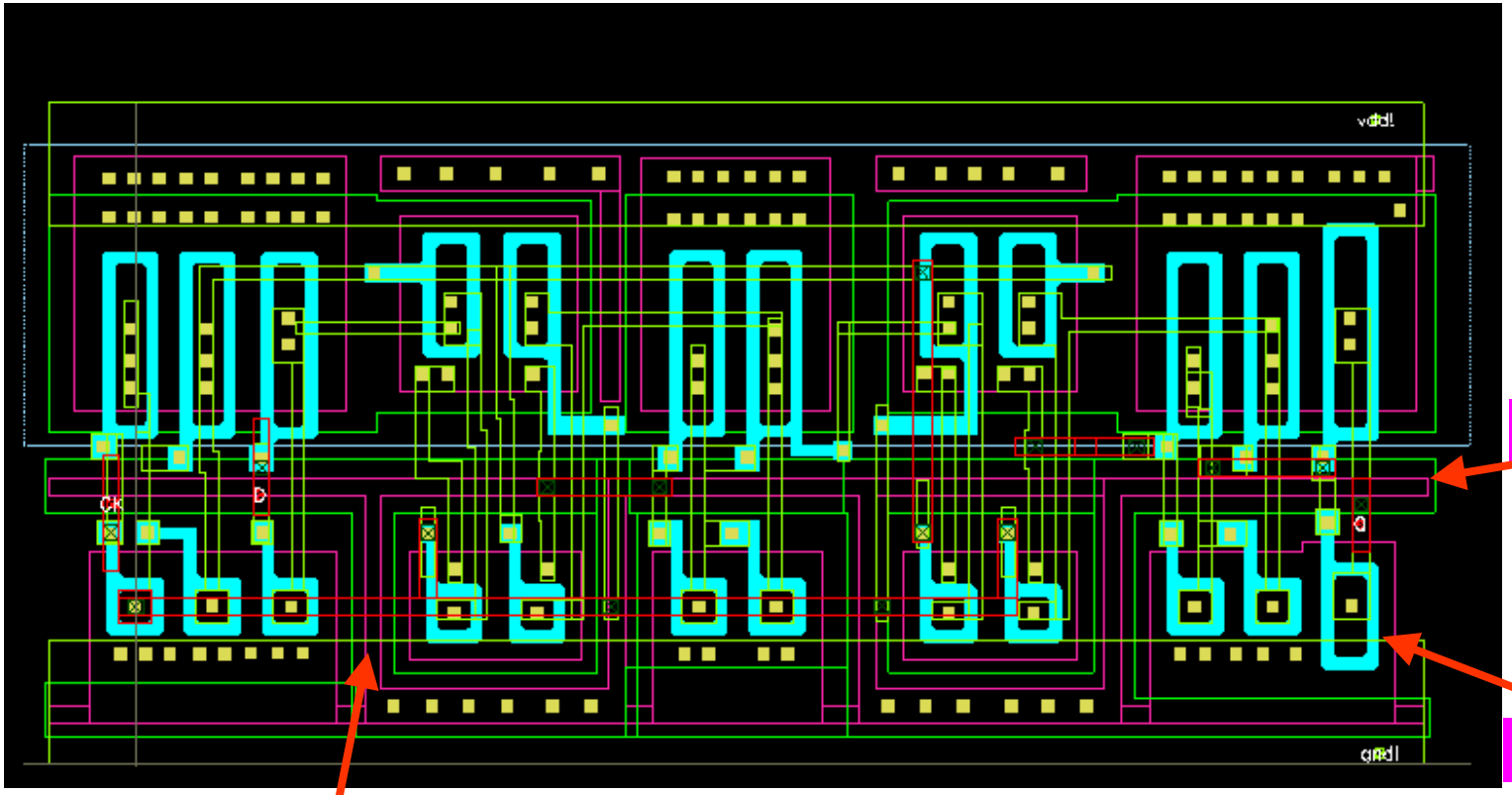


- Designed in ¼ µm CMOS
  - ~ 2x2 mm^2
  - I2C Interface
  - < 10 mW
  - 100 µsec/conversion

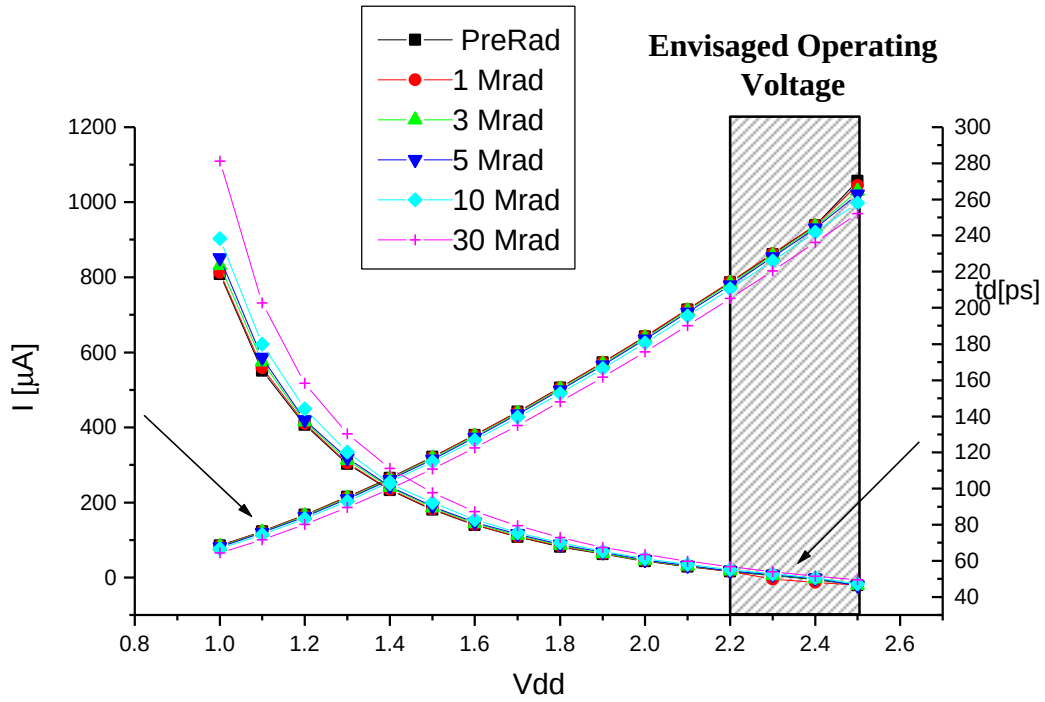
Timing Distribution: PLL-Delay



Library for digital designs



Digital Library Features



1001 Elements Ring Oscillator in 0.25 µm

Power: 0.05 µW/gate*MHz @ 1 V

0.25 µW/gate*MHz @ 2.5 V

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LAN Protocol

- Inspired by Token-Ring
- Can work with single master and “simpler” slaves
- Extensible to any local protocol (I2C. Memory, etc.)
- Max data rate: 32 Mbit/sec

LAN Protocol (1)

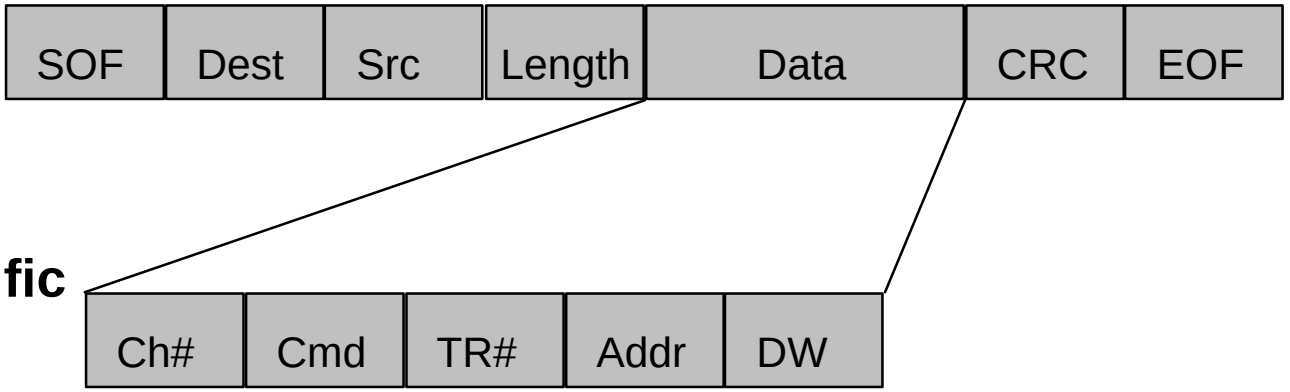
- Ring-like topology
  - Circulating token indicates bus available
  - Source node waits for token:
    - » Removes token, inserts data packet
  - Packet circulates, passed by all nodes
  - Destination copies packet, sets “S” symbol
  - Packet returns to source, is removed by source
  - Source node inserts new token

LAN Protocol (2)

- All nodes can generate packets
- For simplicity:
  - Only the FEC can perform network supervision
    - » Inserts first token
    - » Monitors token integrity
    - » Receives all data packets from CCUs
- FEC requires CPU for protocol management

LAN Protocol: Packet Format

Universal



(Example for an I2C byte write)

LAN Protocol (3a): Write Example

- Transaction sequence:
  - FEC sends command packet
  - CCU receives packet and sets “S” symbol
  - Command packet returns to FEC
  - CCU directs data portion to channel
  - Channel performs action
  - Channel sends ACK packet to CCU specifying TR#

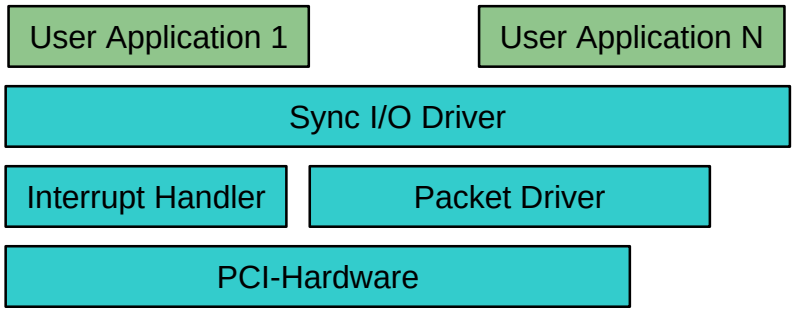
LAN Protocol (3b): Read Example

- Transaction sequence:
  - FEC sends command packet
  - CCU receives packet and sets “S” symbol
  - Command packet returns to FEC
  - CCU directs data portion to channel
  - Channel performs read action
  - Channel sends data back to CCU specifying TR#

LAN Protocol (4): Addressing

- CCU Address allocation
  - FEC has address 0x00
  - Special Broadcast class: 0xf_
  - Up to 254 CCUs on ring
- Channel Addressing
  - » 0: CCU Node controller
  - » 1-15: I2C channels
  - » 16-31: memory channels
  - » 32-47: PIO channel (e.g. HV switches)
  - » 48-63: Event memory controller

Software Architecture



- Lynx-OS
- WinNT
- Linux ?
- Features:
  - Multi-User
  - Multi-Task
  - Synchronous (wait for Ack.)

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Project Status: Hardware

- FEC: PCI-PMC version exists using FPGAs
- CCU: rad-soft, 6 I2C channels, 0.6 μm CMOS version is fully functional
  - Currently being remapped to ¼ μm technology, submission ~ Q1 '01
  - Full ASIC > 250,000 gates
- PLL: exists and is OK in ¼ μm CMOS
- DCU: design ready for submission Q1 '00
- RX40: exists in ¼ mm, design OK
- Laser Driver: rad soft OK, RH submission Q1 '00
- Cost: components well within requirements

Project Status: Software

- You always end up needing more software than you expected
- Low level routines: OK
- Partitioning architecture: work started
- Performance under WinNT:
  - 200,000 I2C transactions/sec (limited by I2C, polling)