First results of the ECS to FrontEnd interface questionnaire

André Augustinus

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Response

The questionnaire has gone out early November.

By now reactions from all subdetectors and some other subsystems:

- full answer from all subdetectors except
  - inner tracker (‘*too early*’)
  - RICH (*~tomorrow*)
- full answer from Readout Unit and magnet.

Thanks ! (but I will keep on bothering you)

Results

CS tasks:

initialisation

loading parameters

loading FPGA’s

status monitoring

calibration

debugging

Some Numbers

ome ideas concerning number of boards and crates:

on detector: >5000 boards

on/near detector: >150 crates

behind the wall: ?

Technical Aspects

terfacing:

I2C (configuration of chips)

JTAG (loading of FPGA's, board testing, parameter loading)

no other 'definitive' choices,

but a lot of suggestions and/or investigations:

- PCI, serial, CAN, I/O lines

Technical Aspects

ome CPU, FPGA availability

elftest:

- JTAG
- write+readback tests

o very strong space/radiation etc. constraints (yet).

Functionality and Performance

/pical configuration:

1 up to few hundred bytes/board

)okUp Tables:

few up to few hundred kbytes/board

PGA loading:

few hundred kbytes up to few Mbytes

some boards maybe grouped

Functionality and Performance

me constraints:

FPGA downloads > 1 min.

LUT loading ~seconds (< 1min)

loading in general only necessary once per run or fill.

Functionality and Performance

onitoring:

very few active monitoring (yet)

small amounts of data (few bytes)

infrequent dumps of data (order of Mbyte

ther:

calibration mode

board tests

“reset”

What next

hort term:

write down requirements (*URD like*) extracted from current answers

get back to people to refine the data

continue investigations in collaboration with IT/CO

onger term:

guidelines, tests, ...