CERN/LHCC 2002-011
April 5, 2002

Review of the LHCb Online System Technical Design Report

1 Introduction

This document describes the process and conclusions of the review of the LHCb Online System. The Online System includes the Data Acquisition System (DAQ) and Experimental Control System (ECS).

The LHCb Data Acquisition System interacts with a four-level (L0 – L3) trigger system:

- to acquire data from the front-end electronics, which receives data at the 40 MHz bunch crossing rate,
- to assemble complete events in a L2/L3 processor farm at 4 GB/s, and
- to send selected events to permanent storage at a nominal event rate of 200 Hz or data rate of 40 MB/s.

The Experiment Control System configures, controls, and monitors the DAQ, the detectors and the whole experimental infrastructure and exchanges information with the LHC, the safety system, and the offline system. The data (DAQ) and control (ECS) paths are separated, and each system is partitioned to support parallel and independent data-taking activities for detector subsystems.

The TDR was received on 19 December 2001 (CERN/LHCC 2001-040). On 21 January 2002, the referees and a consultant discussed the document with the collaboration. The open presentation was given to the LHCC session on 23 January. Following the LHCC meeting the LHCb group received a number of questions. The LHCb collaboration provided a written response to these questions. A discussion of the response and milestones with the referees and the consultant took place on 11 March. The consultant was J.-J. Blaising, and the referees were D. Cassel, F. Ferroni, and Y. Karyotakis.

2 System Technology

The principal elements and technologies of the DAQ system include:

- The Timing and Fast Control system which includes a Timing, Trigger, and Control (TTC) system, a Readout Supervisor (RS) and Throttle switches (to inhibit L0 or L1 triggers). Although the TTC is a general LHC module, it is used in a special mode to synchronize two trigger levels (L0 and L1). The RS is implemented in FPGA.

- A Front End to Gigabit Ethernet interface developed by ATLAS.
- Front End Multiplexers (FEM) and Readout Units (RU). Functional prototypes implemented in FPGA exist and LHCb is keeping this solution as a backup, while it develops a new solution based on Network Processors (NP). The NP solution has several advantages: it provides substantial uniformity and flexibility, programming is relatively easy, simulation and debugging tools are available, and NPs are now standard – they are widely used in network devices and are produced by several companies.
- The Readout Network (RN) which provides connectivity between the RUs and the Sub-Farm Controllers (SFC) with a bandwidth ~ 4 GB/s to ensure that all data arriving at RUs can be passed on to the SFCs without data losses. The technology choice between commercial switches and switches based on NPs has not yet been made.
- Sub-Farm Controllers which assemble data arriving from the RUs to form complete events, isolate the readout network from the sub-farm computing systems, and balance loads among the sub-farm processors. The SFCs are connected to the RN via a "smart NIC" (Network Interface Card) which also performs the final event building.
- The Event Filter Farm which consists of many CPUs organized into sub-farms, each of which receive events from a Sub-Farm Controller.

The DAQ system is scalable because it is parallel; there is no synchronization or communication between components at the same level or at different levels, and there is no central event builder. Data are transferred between stages in a "push protocol", *i.e.*, each module or stage with data will immediately push the data to the next higher level. With this protocol and the parallel architecture, data rates need not be limited by the bandwidths of the links between stages, but by the amount of buffering at each stage. Hence, buffering is matched to anticipated data rates at each stage and unusually high rates are handled by throttle control of the L0 and L1 triggers.

The ECS consists of a small number of high end server PCs on the surface connected to a large disk server for the detector configuration data base, archives, log files, etc. These servers communicate with other systems (such as the LHC and safety) and with hundreds of PCs in the counting rooms which interface to the experimental equipment. The software architecture is a hierarchical, tree-like, structure, which represents the structure of subdetectors, subsystems, and hardware components. This hierarchy allows substantial independence among components while enabling integrated automated and user-driven control.

For interfaces in regions near the detector where radiation tolerance is essential, the ECS utilizes Serial Protocol for Experimental Control System (SPECS) slaves or the ATLAS Embedded Local Monitoring Box (ELMB). In the counting rooms where radiation is not an issue, Credit-Card PCs (CC-PC) are used. The ECS software is based on the LHC-wide Joint Controls Project (JCOP) framework. This framework allows the integration of all components in a coherent system which preserves

partitioning. Overall, the ECS system design guarantees operational independence of control of the data flow, the detector, and infrastructure.

3 Comments

The LHCC finds the detector technologies adopted for the Online System (Data Acquisition System and Experiment Control System) adequate to achieve the physics goals stated in the Technical Proposal, and **congratulates** the LHCb collaboration for the quality of work presented in the TDR.

Although there are no major concerns, the LHCC notes that:

- At present only about half of the required manpower is available. The Committee asks the LHCb Collaboration to submit a written plan describing how the missing manpower will be secured.
- Finding and engaging personnel with the expertise required to design the Network Processor board is essential.

The LHCC recommends that LHCb follows the established practice of conducting independent reviews of the engineering designs.

A list of agreed milestones to monitor and regulate the progress of the project is appended.

Online System Milestones

Experimental Control System	
ECS electronics interfaces prototypes ready	Apr 2002
ECS electronics interfaces finalize design	Dec 2002
ECS software framework first release	Jun 2002
Timing and Fast Control	
TFC prototypes ready	Jan 2003
TFC production start	Aug 2003
Network Processors	
NP-based RU prototype ready	Jun 2003
Readout Network implementation decision	Sep 2003
NP-based RU production start	Oct 2003
Installation and Commissioning	
Start installation in Pit 8	Oct 2003
Start commissioning	Jan 2004