Status of the LHCb upgrade

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1 Introduction

The LHCb upgrade, as described in the Letter of Intent (LoI) [1] and Framework Technical Design Report (TDR) [2], is progressing according to schedule. Two major decisions on technology choices took place in June 2013, namely for the Vertex Locator (VELO) and for the ring-imaging Cherenkov (RICH) detectors. This will allow the TDRs to be submitted for the VELO and particle identification detectors (RICH, Calorimeter and Muon systems) by December 2013. Another decision, on the choice of technology for the main tracking stations, is due in November 2013, and will be followed by the TDR for the tracking system (Upstream Tracker and Main Tracker) in March 2014. Thus by April 2014 the detailed cost breakdown for all detector components will be available, as well as the sharing of responsibilities among the involved institutes. Negotiations with the funding agencies are also progressing well, for covering the expected CORE contributions to the various sub-detector components to which the participating institutes have committed. Activities over the last six months have allowed the performance of the upgraded detector to be further optimized, and the collaboration is determined to develop and construct the upgrade detector within the cost envelope given in the Framework TDR, to be ready for installation during an 18 month-long shutdown (LS2).

The physics programme of the LHCb upgrade has been described in the LoI [1] and Framework TDR [2], with more detailed discussion in a dedicated paper co-authored by the LHCb collaboration and theorists [3]. However, work has been ongoing to refine the studies as more detailed descriptions of the upgrade detector are implemented in simulation. A document entitled "Impact of the LHCb Upgrade detector design choices on physics and trigger performance" was prepared to support the VELO upgrade technology review. An updated version of this document will be made publicly available around the end of the year to support the sub-detector TDRs. As an intermediate step, in the context of the ECFA High Luminosity LHC Experiments Workshop, updated sensitivity projections have been prepared (see Table 1) based on the latest information from analyses of data collected during the LHC Run 1 and for the expected evolution of the trigger efficiency [4]. The comparison of the sensitivity projections with those for Heavy Flavour

Table 1: Statistical sensitivities of the LHCb upgrade to key observables. For each observable the expected sensitivity is given for the integrated luminosity accumulated by the end of LHC Run 1, by 2018 (assuming $5\,\text{fb}^{-1}$ recorded during Run 2) and for the LHCb Upgrade ($50\,\text{fb}^{-1}$). An estimate of the theoretical uncertainty is also given.

Type	Observable	LHC Run 1	LHCb 2018	LHCb upgrade	Theory
B_s^0 mixing	$\phi_s(B_s^0 \to J/\psi\,\phi)$ (rad)	0.05	0.025	**0.009**	~ 0.003
	$\phi_s(B_s^0 \to J/\psi\,f_0(980))$ (rad)	0.09	0.05	**0.016**	~ 0.01
	$A_{\text{sl}}(B_s^0)$ (10^{-3})	2.8	1.4	**0.5**	0.03
Gluonic penguin	$\phi_s^{\text{eff}}(B_s^0 \to \phi\phi)$ (rad)	0.18	0.12	**0.026**	0.02
	$\phi_s^{\text{eff}}(B_s^0 \to K^{*0}\bar{K}^{*0})$ (rad)	0.19	0.13	**0.029**	< 0.02
	$2\beta^{\text{eff}}(B^0 \to \phi K_S^0)$ (rad)	0.30	0.20	**0.04**	0.02
Right-handed currents	$\phi_s^{\text{eff}}(B_s^0 \to \phi\gamma)$	0.20	0.13	**0.030**	< 0.01
	$\tau^{\text{eff}}(B_s^0 \to \phi\gamma)/\tau_{B_s^0}$	5%	3.2%	**0.8%**	0.2%
Electroweak penguin	$S_3(B^0 \to K^{*0}\mu^+\mu^-; 1 < q^2 < 6\,\text{GeV}^2/c^4)$	0.04	0.020	**0.007**	0.02
	$q_0^2\,A_{\text{FB}}(B^0 \to K^{*0}\mu^+\mu^-)$	10%	5%	**1.9%**	$\sim 7\%$
	$A_{\text{I}}(K\mu^+\mu^-; 1 < q^2 < 6\,\text{GeV}^2/c^4)$	0.14	0.07	**0.024**	~ 0.02
	$\mathcal{B}(B^+ \to \pi^+\mu^+\mu^-)/\mathcal{B}(B^+ \to K^+\mu^+\mu^-)$	14%	7%	**2.4%**	$\sim 10\%$
Higgs penguin	$\mathcal{B}(B_s^0 \to \mu^+\mu^-)$ (10^{-9})	1.0	0.5	**0.19**	0.3
	$\mathcal{B}(B^0 \to \mu^+\mu^-)/\mathcal{B}(B_s^0 \to \mu^+\mu^-)$	220%	110%	**40%**	$\sim 5\%$
Unitarity triangle angles	$\gamma(B \to D^{(*)}K^{(*)})$	7°	4°	**1.1°**	negligible
	$\gamma(B_s^0 \to D_s^{\mp}K^{\pm})$	17°	11°	**2.4°**	negligible
	$\beta(B^0 \to J/\psi\,K_S^0)$	1.7°	0.8°	**0.31°**	negligible
Charm	$A_\Gamma(D^0 \to K^+K^-)$ (10^{-4})	3.4	2.2	**0.5**	–
CP violation	ΔA_{CP} (10^{-3})	0.8	0.5	**0.12**	–

observables from ATLAS, CMS and Belle II confirms that the LHCb upgrade will be the world's leading heavy flavour experiment in the next decade.

In the following we give a brief update on the R&D activities for the tracking and particle identification detectors, and discuss the choice of the technological options for the VELO and RICH systems. The status of track reconstruction and data processing are reviewed, as well as the progress in preparing for the LHCb upgrade in terms of interaction with the LHC machine groups, infrastructure, schedule and funding.

2   Tracker system upgrade

Considerable progress has been achieved towards a decision on the technological choices of the tracker system upgrade. For the Vertex Locator (VELO) the pixel layout with microchannel CO_2 cooling has been adopted. Concerning the options of an enlarged Inner Tracker (IT) with Outer Tracker (OT) straw tubes, or building the main tracking stations with a new scintillating fibre technology, a major step forward has been achieved in qualifying the fibre technology for the radiation requirements in the upgrade conditions. Furthermore, simulation studies have shown that building the main tracking stations from a full Fibre Tracker (FT) in combination with a silicon-strip Upstream Tracker (UT), the pattern-recognition performance will allow a fully efficient and flexible software trigger to be run within the expected time constraints of the computing farm.

2.1   Vertex Locator

An important decision was taken end of June concerning the choice of VELO silicon sensors and cooling technologies. This was the result of a detailed review of R&D and performance simulations of the silicon microstrip option versus the silicon pixel option and of two different cooling techniques, a classic substrate versus a microchannel substrate. Results from full-sized strip sensors with good HV tolerance, incorporated into modules and including signal to noise measurements, were discussed. Results were also presented for prototype pixel sensors from three different companies, bonded to electronic chips (Timepix and Medipix ASICs) that were irradiated and operated in test beams. Radiation damage performance results as well as detailed RF-foil designs were implemented in the general LHCb software framework, and high-level trigger (HLT) pattern recognition algorithms and reconstruction timing were worked out in detail. Full software implementation in a complete LHCb upgrade simulation framework was used to demonstrate the benefit of a smaller inner radius (compared to the LoI) for both the strip and pixel options. Physics performance of strips and pixels were shown to be rather similar, however, processing speed, robustness and decreased risk-driving factors finally led to the choice of the pixel design with microchannel cooling.

Since the review, R&D has continued on the microchannel cooling. The design was modified to improve pressure resistance, adapt to a full-scale module, to incorporate a symmetric placement of the connector and to improve the robustness of the collector.

The Timepix3 chip was delivered in August and testing is well underway. A low pixel

noise was measured, the power consumption is within specifications, and the periphery and pixel matrix are fully functional. Excellent linearity was demonstrated. These results, although preliminary, constitute a very encouraging step towards the Velopix, an evolution of the Timepix3 chip. Recently, the VELO group has decided to simplify the Velopix readout architecture and to mitigate the risk of a possible delivery delay, by choosing a binary readout that provides more speed at essentially equivalent physics performance.

Important new results were obtained on the RF foil fabrication. Tests were conducted to see if a complex, corrugated foil of 0.3 mm thickness could be post-processed by chemical etching in order to achieve a reduced thickness in selected regions of the foil of order 0.15 mm. First promising results were obtained on an L-shaped sample of about 20×20 cm^2, and preliminary results show good thickness homogeneity and vacuum-tightness.

2.2   Upstream Tracker

The Upstream Tracker (UT) design is based on the stave concept described in the LoI [1], with active cooling embedded in a carbon foam support structure that hosts hybrid circuits providing the electrical connectivity of the silicon front-end electronics elements to the back-end electronics. R&D has started to test various aspects of the most critical inner silicon-sensor design close to the beam pipe. Full-sized sensors with 5 cm strips are being produced that can be daisy-chained, as well as smaller detectors to test the procedure to cut the hole near the beam pipe and to study the guard-ring design. In this development, a number of mechanical prototypes of thickness equal or smaller than the planned one will be produced, so that full-scale mock-ups can be assembled with the right mechanical properties.

The UT is readout by a custom made electronics chip, the so-called "SALT chip". The status of this chip is discussed in Section 2.4. The electronics readout architecture and data formatting has been defined, and the components that need to be constructed to test the UT readout slice were identified. A test stand is being configured and will be used for system tests. Progress was made towards the construction of a full size mechanical mock-up with embedded cooling, for which a prototype CO_2 cooling system is being built. A conceptual design review of the Upstream Tracker and an electronics architecture review are planned for November this year.

2.3   Inner Tracker

For the option of an enlarged Inner Tracker (IT) silicon microstrip detector, two mechanical prototype ladders have been produced. Their stiffness and natural vibration frequency have been measured to be within specifications. The very light and innovative carbon-roving support of a ladder increases the total material budget by less than 5%. Simulating the Outer Tracker (OT) performance with this reduced mass and increased size of the IT shows that the tracking efficiencies in the OT remain sufficiently high, even up to luminosities well beyond 2×10^{33} cm^{-2}s^{-1}.

A cooling demonstrator set-up has been manufactured, representing $\sim 10\%$ of the envisaged size and power dissipation of an IT station. Tests show that the sensors close

to the beam-pipe can be maintained well below the required temperature of $\sim 5\,°\mathrm{C}$. The mechanical design of the IT boxes has been changed to allow cooling the sensors with cold air while cooling the FE-electronics at room temperature. A set-up has been made to perform a final test, measuring the vibration of the mechanical modules in the required airflow, which now is reduced to a minimum due to the improved box design.

2.4   Silicon strip ASIC (SALT chip)

The readout chip for both the Inner Tracker option and for the Upstream Tracker is the SALT chip. Since February 2013, the following R&D was carried out for this chip:

1. First submission of the analogue front-end (FE) part with 8 channels;

2. First submission of the single-to-differential (S/D) converter;

3. Tests and performance analysis of a single ADC channel and the PLL block (8 channels);

4. Testing commenced of the front-end and S/D converter;

5. Digital signal processing (DSP) chain defined, first version of stand-alone emulation software has been finished.

Progress regarding tests of the ADC and PLL circuit has been presented at TWEPP 2013.
   In the coming six months intensive testing of existing prototypes and preparation for the next submissions will continue. The plan is to submit an 8-channel FE with ADC in February 2014. The low-level DSP chain emulation model and preparation of the high- and low-level emulation software will be implemented.

2.5   Outer Tracker

In view of the scintillating fibre technology being the current baseline option with a technical review in November this year, R&D for an Outer Tracker straw-tube upgrade with shorter straw-tube modules and 40 MHz electronics readout has at present no longer been pursued in any of the collaborating institutes. While awaiting a final technical decision, all straw-tube module production tools have been preserved, as well as the functional prototypes of the upgraded straw-tube electronics.

2.6   Fibre Tracker

The study of the Fibre Tracker (FT) has evolved positively over the last six months and its scope has been extended to a Full Tracker option, which is conceived to completely replace the current Inner and Outer Tracker stations.
   The general viability of a large scintillating-fibre based tracker with silicon photomultiplier (SiPM) readout was demonstrated in the review in February, and has been further consolidated by new fibre irradiation results (up to two times the expected dose) and

also lab measurements on new and improved SiPM prototypes. We currently pursue an R&D programme with two companies providing the SiPMs. Detectors with a new design are currently under production. The optimized design should lead to further progress in terms of cross-talk probability and photon detection efficiency and in the end result in an increased performance margin of the fibre tracker. Effort has been spent on developing the expertise and equipment to produce large-size fibre modules (from 1 to 2.5 m length): winding, casting, cutting, aligning, and assembling on light support structures. While the fabrication of the first prototype module is imminent, several modules of different geometry will be built for a variety of structural and readout tests. Major progress was achieved in the definition of the front-end electronics, where the required functionality may be split-up between a new ASIC, the so-called PACIFIC chip, and commercial FP-GAs. Essential parts of the ASIC were simulated and its design is in an advanced state. The SiPMs require to be operated at low temperature ($-40\,^\circ$C) to compensate for the increased noise rate due to radiation damage. In addition to establishing a detailed thermal model, the suitability of several cooling options was studied in lab set-ups with realistic thermal mock-ups.

Finally, hand-in-hand with the hardware work, the Monte Carlo simulation and the tracking codes are being refined. A reliable detector model is the basis for realistic performance assessments and further design optimizations. The team, enhanced by several collaborating institutes recently joining the effort, will focus on the definition of the essential parameters of a baseline design and, wherever possible, a verification of its critical aspects. This will be the basis of the TDR which is due in March 2014.

3   Track reconstruction

In the last six months the geometry descriptions of all tracking detectors have been finalized and all pattern recognition algorithms have been adapted to the upgrade environment. The overall performance in terms of efficiency, ghost rate and timing, running under upgrade conditions, is the same or even better than the performance of the current detector in the current running conditions. No show-stopper has been found for any of the potential upgrade tracking detector designs. Dedicated efforts have been made in the following areas:

1. **Input to the vertex detector technology choice in May 2013**
   The geometries of several different detectors have been studied: a pixel and a strip detector both with two cooling options (different amount of material and thus multiple scattering) and both in the nominal and compact design (reduced distance of active area to the interaction point). While the strip detector resulted in a slightly better impact parameter resolution, the pixel detector showed significantly better performance in efficiency, ghost rate and timing and an impact parameter resolution at least as good as the current detector. The choice of the cooling option had hardly any impact on the performance while the compact design improved the impact parameter resolution. Thus the pixel detector with the compact design was chosen as vertex detector for the upgrade.

2. **Robustness studies for the Fibre Tracker**
   One concern of the referees from the review of the fibre tracker was the robustness of the seeding (T station standalone) algorithm in non-ideal conditions. As the design of the fibre tracker (contrary to the current forward spectrometer) foresees no segmentation in the y (vertical) direction the combination of x and stereo layers hits results in a large number of possible 3D measurements. This is especially true if the distance between the x and stereo layer is large and the track slope unknown, as in case of the seeding algorithm. Detailed studies of the mono-layer design (larger distance between x and stereo layers compared to the original bilayer design) including worst-case estimates of dead regions, photon yields and noise demonstrated very stable performance for all pattern recognition algorithms on data samples generated with a pile-up corresponding to up to $\nu = 11.4$ (more than 30% above the design goal of 2×10^{33} cm^{-2}s^{-1}).

3. **Occupancy studies for the IT option**
   The alternative design to the Fibre Tracker is an enlarged silicon detector (IT) near the beam pipe and straw tube detector modules (OT) outside. As this design is conceptually very similar to the current forward tracking system, the according performance studies have been up to now limited to check that the proposed IT surface is sufficiently large and the material budget sufficiently low to ensure that the occupancies in the OT are comparable or lower than in the current running conditions.

4. **Track reconstruction for the trigger**
   The main algorithm to reconstruct long tracks (tracks with measurements in the vertex detector and the T stations) is the forward algorithm, a Hough transformation approach which extrapolates track segments reconstructed in the vertex detector to the T stations. Studies with the full simulation revealed that the forward algorithm in the upgrade detector is significantly faster ($\times 5$) than the current version of the algorithm on the current detector, despite the higher luminosity. This is mainly related to the excellent resolution of the fibre tracker without any need for resolving drift-time ambiguities (compared to the OT). An additional approach to speed up the forward pattern recognition even further is to get a fast momentum estimate by combining VELO tracks with UT measurements and then limit the search of the forward algorithm accordingly to a restricted range in the T stations. This approach did not work for the current detector due to the limited TT acceptance. Initial studies of the VELO+UT algorithm indicate a further gain in timing of a factor 2–3. As the long-track reconstruction was up to now the limiting factor for the HLT we could only afford to pass selected vertex detector tracks with a large impact parameter to the forward algorithm in the trigger. The new fast algorithms for the upgrade open the door to new approaches. It is especially attractive to run the forward tracking on all vertex detector tracks and thus to reproduce exactly the offline running scenario in the trigger.

4 Particle identification system upgrade

Since the last report major decisions have been taken for each of the three particle identification (PID) sub-detectors. Although several questions are still open, it is realistic to aim for a common PID TDR to be submitted in time for consideration at the December LHCC meeting.

4.1 RICH system

A critical decision for the upgraded PID system was taken in June, when the collaboration endorsed a recommendation from the RICH group to choose a redesigned RICH 1 as the optimal solution for coping with the demands of operation at higher luminosity. This option was preferred over an alternative proposal in which RICH 1 would be removed entirely and RICH 2 would be replaced by a two-radiator detector. The key feature of the new RICH 1 is a modification of the optics (and hence also the mechanics of the gas vessel) in order to spread the image more with respect to the current detector, and thereby reduce occupancy. This re-design can however be performed within the footprint of the current RICH 1, and therefore is compatible with the existing magnetic shielding box, and the evolving plans of the VELO and the UT. Simulation indicates that the physics performance of the new RICH system at high luminosity will be very similar to that achieved with the existing detector in LHC Run 1.

The multianode photomultiplier is established as the baseline technology for the RICH photodetector. Studies are now being completed concerning ageing and magnetic field tolerance, and the results obtained so far are satisfactory. The final test will be to read out the photodetector at 40 MHz. An electronics review in early October established the CLARO chip as the baseline for the front-end, but its radiation tolerance with incident protons still needs to be quantified.

4.2 Calorimeter system

The existing electromagnetic and hadronic calorimeters will remain, but the Scintillating Pad Detector and Preshower will be removed, as they are considered inessential for the most important calorimeter-based physics topics of the upgrade, such as radiative penguin studies, and will no longer be required for the trigger. Simulation studies are now advanced to investigate the offline performance of the upgrade calorimeter system at high luminosity. Changes to the clustering algorithm and cluster definitions are found to be effective in combatting the effects of pile-up.

An important decision taken since the last report concerns the lifetime of the modules in the hottest part of the inner region. Results drawing on radiation tests from test modules in the tunnel itself, and from a module exposed in the PS IRRAD facility, led to the conclusion that the current modules will be able to survive until LS3. Not needing to perform any replacement during LS2 is beneficial for the scheduling of other upgrade work during this period. Spares already exist for the replacement, and the procedure for making the exchange will be outlined in the TDR.

The principal challenge in the calorimeter upgrade lies in the front-end electronics, which must read out at 40 MHz, and cope with the five-fold reduction in gain that will be applied to the PMTs. Maintaining the noise level of the analogue components under these requirements is a demanding task, and two solutions are being considered and prototyped, one ASIC-based and the other making use of discrete components. A decision between the two options will be made when the final ASIC prototype is available in the new year, a time-scale which is compatible with that required for the final electronics design.

4.3 Muon system

Based on tests at high luminosity and results from ageing tests it has been decided that no new detectors will be needed in the hottest regions of the first two upgrade stations until after LS3. Nevertheless, work is already underway in defining the technology for these new detectors, with triple GEM and cathode-readout MWPCs being the chosen solutions for innermost and next-to-innermost regions, respectively. However, the realization that the existing technology will be sufficient for the post-LS2 run allows attention to be focused on other aspects of the upgrade. The general architecture of electronics for the post-LS2 detector is now settled, and a recent workshop focused on specific implementation issues. Here there is a close coupling with the trigger, and hence certain decisions concerning the low-level trigger will not be taken until the trigger TDR of next year.

5 Data processing

The task of the data processing concerns the transport of the data from the output of the front-end electronics up to their reconstruction. It encompasses data acquisition, trigger and computing.

5.1 Data acquisition

Four of the sub-detector readout architectures have been reviewed, and the remainder (VELO, UT and FT) will be scrutinized in November/December.

Several scenarios are under study to determine the best location of the readout electronics. The preferred one is when the readout electronics is close to the network switches in a building located on the surface. The performance of the long-distance optical link between the underground area and the surface, as well as the details of the installation procedure, show that this is feasible at an affordable cost. The decision will be taken at the end of 2013.

Prototyping the 40 MHz readout unit is progressing well. Several readout boards (AMC40) have been distributed to the collaboration in order to acquire data from the sub-detector prototypes. A second version is in preparation to improve the buffering capabilities by a large factor.

The 40 MHz event building is performed by a mixture of large-scale computing network and CPUs. The main challenge is to find a cost-effective solution which can handle a

bandwidth of 32 Tbps. The solution envisaged in the Framework TDR is similar to the current LHCb system but with a much larger bandwidth. It is based on 10 Gb Ethernet links and several fat-core routers with a large amount of internal memory to handle traffic congestion. The new building at the surface opens the road to an attractive approach where the readout unit and the CPU running the event builder can be merged in the same entity, a PC server. The data transfer between the PC servers would be handled by a large bi-directional router with input and output ports at 100 Gbps each. A detailed review of the readout architecture including timing and fast command distributions, slow control and low-level trigger is foreseen early in 2014.

5.2 Trigger

Two workshops have been organized to discuss the low-level trigger (LLT) architecture and its performance. The baseline implementation relies on dedicated hardware using the readout unit, but the new approach for the event building opens the possibility to implement it via a software running on the PC servers. More studies are required to understand the CPU load and timing issues.

Concerning the high-level trigger (HLT), the internal document *Upgrade Physics and Trigger* has been published. It describes the HLT efficiencies for several key channels and for different detector configurations running in the upgrade conditions. It has also been shown that the full 40 MHz tracking can be performed in the farm envisaged in the Framework TDR when the detector is made of VELO pixel, UT and the full Fibre Tracker. Studies are ongoing to better understand the combinatorics in the selection as well as the HLT output bandwidth.

5.3 Computing

The computing project has reviewed the existing tools, practices and requirements. The DIRAC and computing infrastructure is well adapted to our needs and no show-stopper has been identified on the scalability. Although it is rather difficult to already define the computing model for 2018, it will rely on the new developments which will be available after LS1 and on a more intelligent data management and replication system.

6 Preparation for the LHCb upgrade

6.1 Interactions with LHC machine groups

In previous reports the importance of taking equal amounts of data with both spectrometer polarities in order to control the systematic uncertainties in the measurement of *CP* asymmetries has been underlined. Until recently it was thought that for 25 ns bunch spacing, as required for the upgrade, this is only possible if the external beam crossing angle is in the vertical plane. To ensure sufficient apertures for injection of the beams in the vertical crossing plane, a rotation of the beam screen in the quadruple magnet Q1 would be needed, as otherwise the crossing plane has to be rotated for each fill when the

maximum beam energy is reached. This issue has been revisited in the past months by machine experts who found an elegant solution which allows for data taking with both LHCb spectrometer polarities, 25 ns bunch spacing and a horizontal external crossing angle. The solution consists in a slightly larger parallel beam separation at injection together with a small vertical crossing angle of the same sign for both beams. The resulting difference between the total crossing angles for the two spectrometer polarities turns out to be about $540\,\mu$rad at 7 TeV beam energy, which does not pose a problem for the physics studies foreseen. Studies are also on-going regarding the frequency of the polarity changes. First indications show that it should be similar as during Run 1, hence about every two weeks.

6.2 LHCb upgrade infrastructure

The installation of the LHCb upgrade is scheduled over 18 months, starting beginning of 2018. As not only several detectors will have to be exchanged, but associated infrastructure as well, the possibility to bring forward some installation is being evaluated. The installation of the support for optical fibres during LS1 has been discussed, but it turned out that fixing of the guide tubes to the shaft walls can be done in a very short time window. Therefore, it has been decided to perform this installation during one of the Winter technical stops closer to 2018. Nevertheless, it is planned to pull a set of fibres for test purposes. It is expected that this installation will show the feasibility of moving the event building and CPU farm to the surface at the experimental site. All consolidation work that is required for the running experiment will be performed, inline with the LHCb upgrade wherever possible.

6.3 Schedule

The first TDRs will be issued in December 2013, for the VELO and particle ID detectors (RICH, Calorimeter and Muon systems). The TDR for the tracker (and possibly for the low-level trigger) is scheduled for March 2014. The milestones that have been defined until the submission of the TDRs have mostly been met. The technology choice for the Vertex Locator and RICH systems has been made and the preparation for the TDRs is in full swing. A review of the tracker system upstream the magnet will take place in November 2013, and the decision on the technology for the tracker system downstream of the dipole has been scheduled for end-November 2013.

There are two options for the event-builder as part of the DAQ, and the baseline for this system will be decided early in 2014. With the technology choice made for the VELO and RICH, the installation schedule for these systems will now be prepared in more detail.

6.4 Funding

Following approval of the Framework TDR [2], the Memorandum of Understanding (MoU) [5] for Common Projects was submitted to the RRB in April 2012. In both these documents the overall cost of the LHCb upgrade was estimated to be 57 MCHF,

including a 30% Common Fund (CF) contribution. Since then, important technological choices have been made and many components of the upgrade detector have been further optimized. Following progress of the last six months we are confident that the upgraded detector with 40 MHz readout and with a fully efficient and flexible software trigger can indeed be constructed and installed within the cost envelope given in the Framework TDR. Any significant reduction of the expected funding would however put the upgrade project at risk, since staging any component of the one-go 40 MHz detector upgrade would jeopardise operation after Long Shutdown 2.

A breakdown of the cost for the different detector sub-systems and the sharing of responsibilities among institutes will be described in detail in the upcoming sub-system TDRs at the end of 2013 and beginning of 2014. Negotiations with the funding agencies for covering the expected CORE contributions to the various sub-detector components to which the participating institutes have committed, are progressing well. Encouraging feedback has been received, covering a large fraction of the requested funds.

References

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